

100

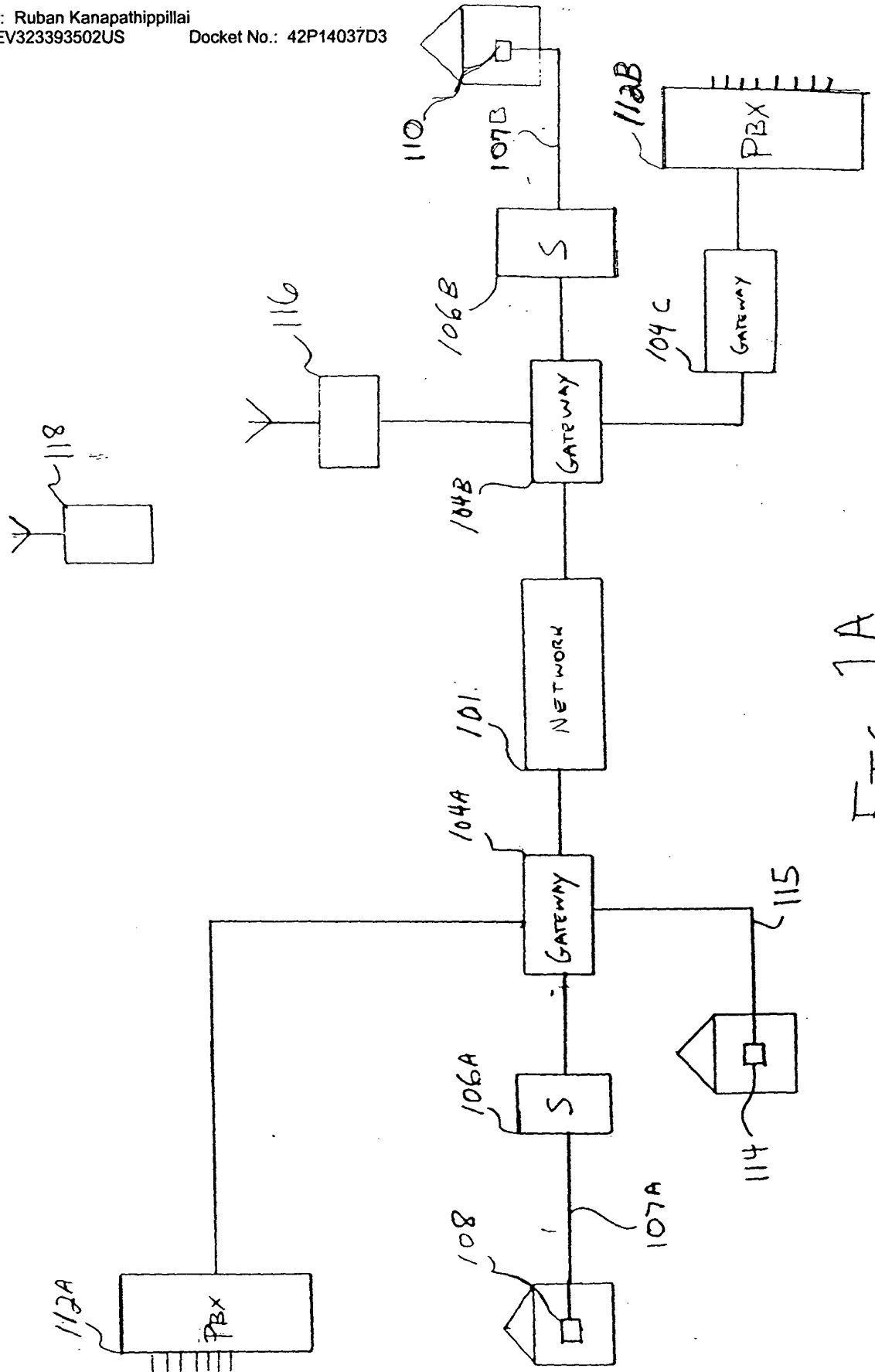


FIG. 1A

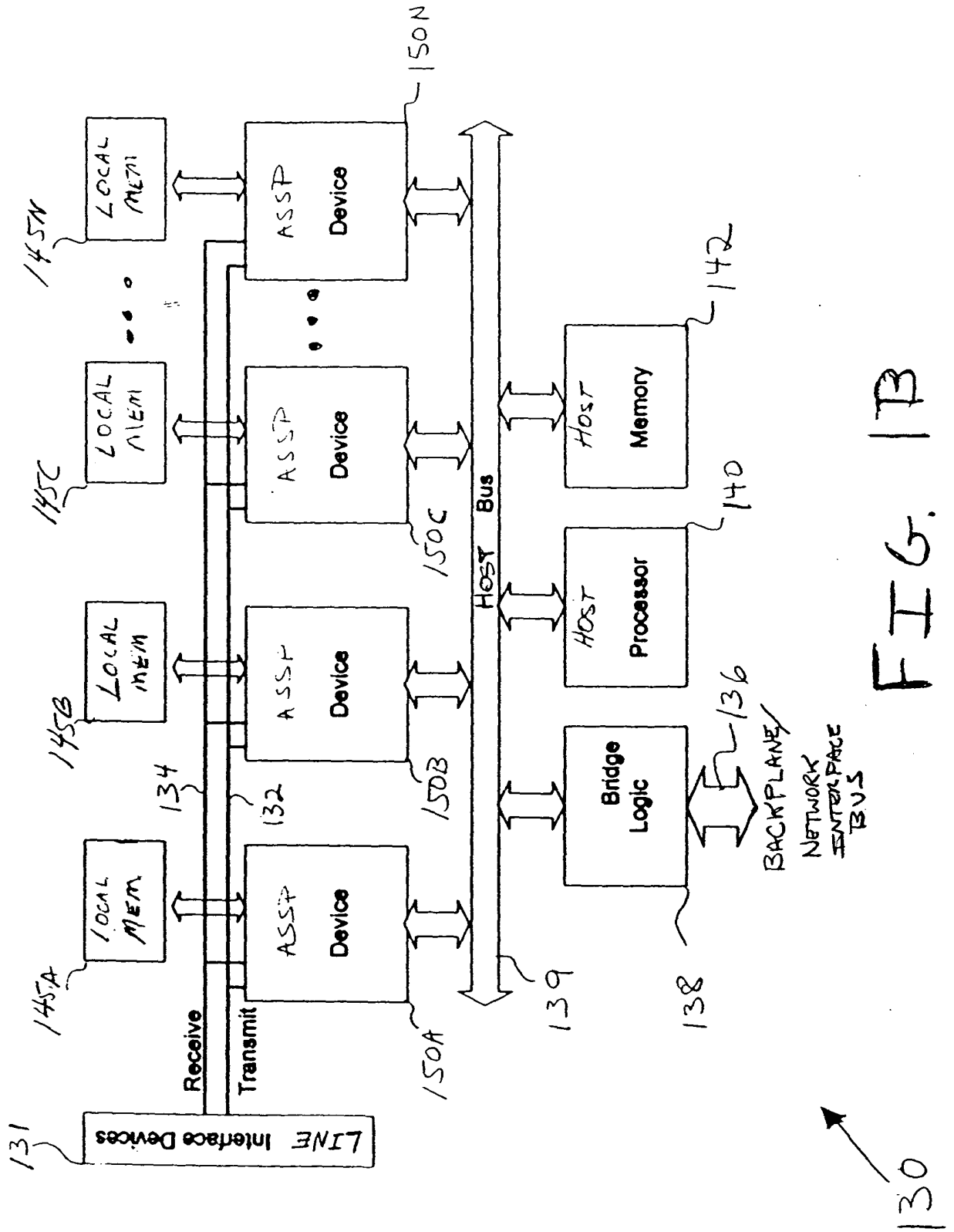


FIG. 1B

150

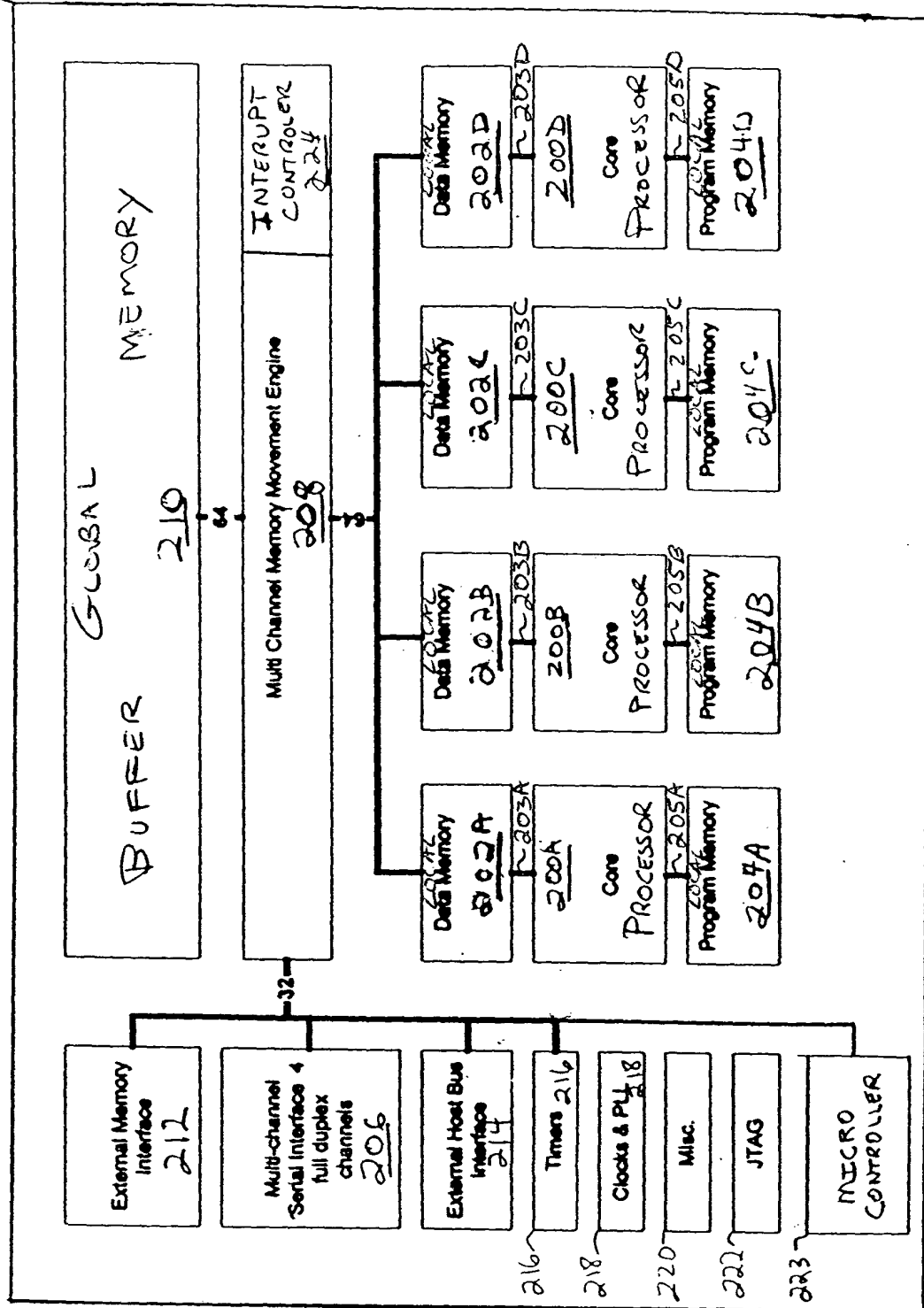


FIG. 2

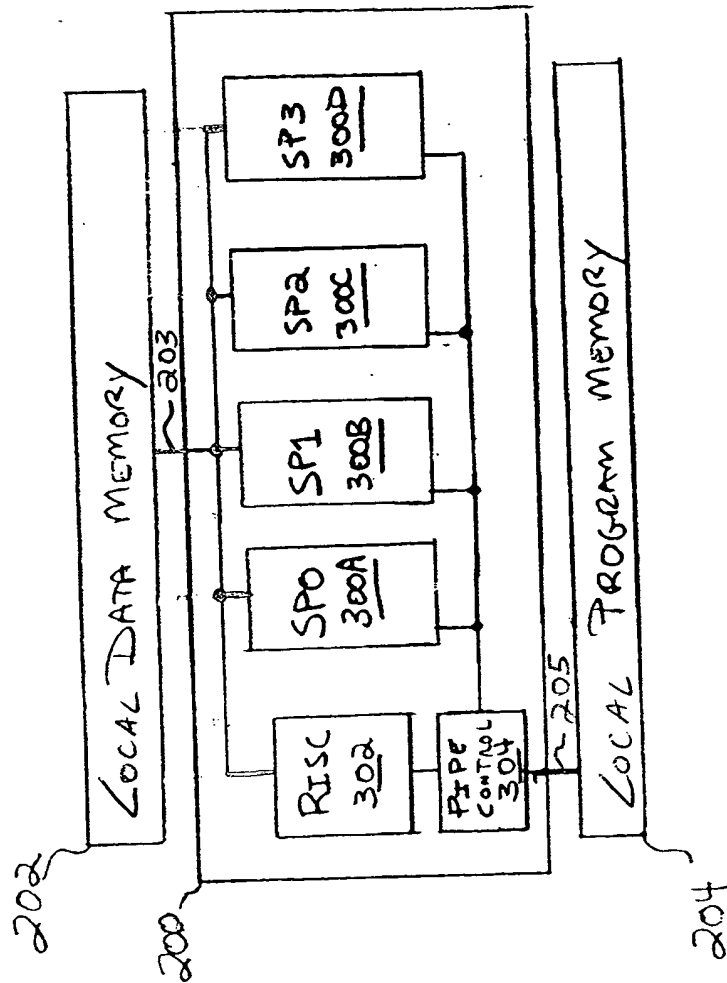


FIG. 3

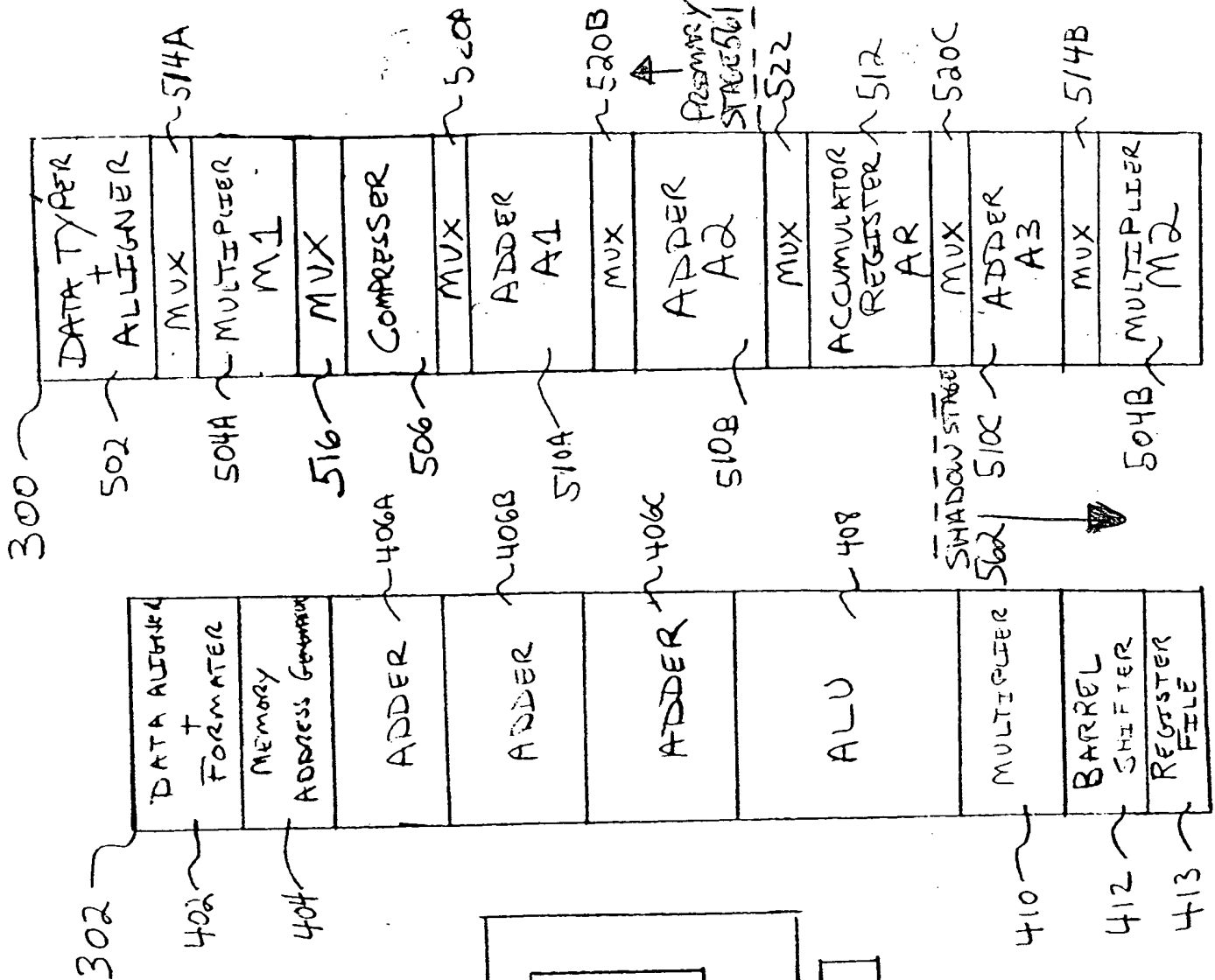


FIG. 4

FIG. 5A

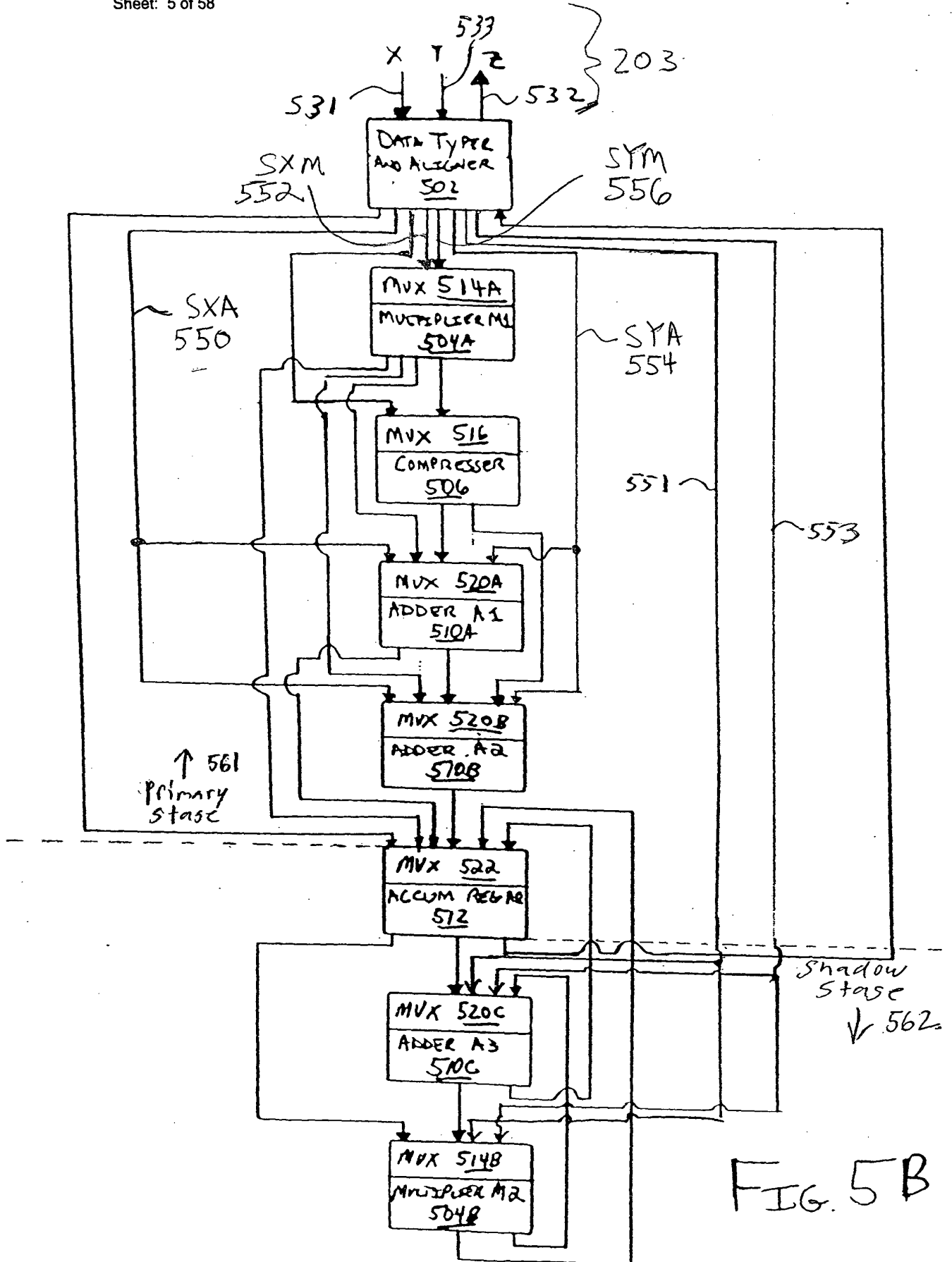


FIG. 5B

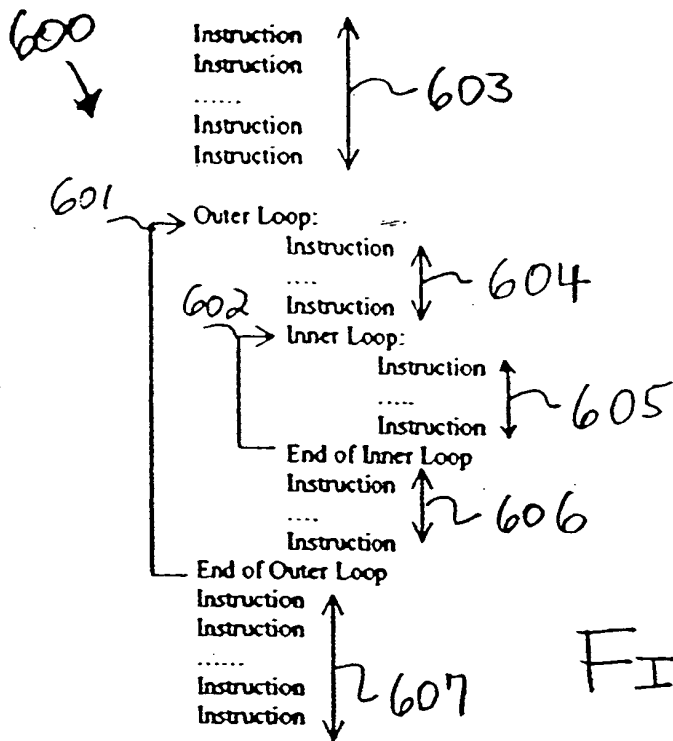


FIG. 6A

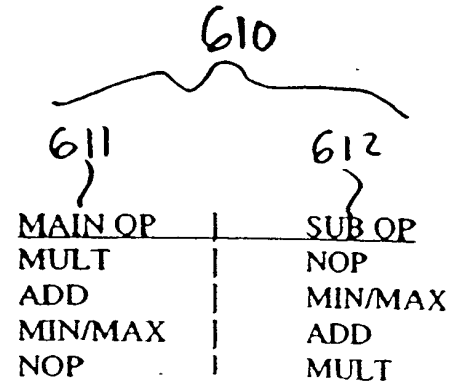


FIG. 6G

20-bit ISA

39	19
0	0
0	1
1	0
1	1

20-bit parallel  
 20-bit serial  
 40-bit extended  
 20-bit serial

Control # Control  
 Control # Control  
 DSP, extensions/Shadow  
 DSP # DSP

FIG. 6B

### 6-bit operand specifier

A 6-bit specifier is used in DSP extended instructions to access memory and register operands.

5	4	3	2	1	0
M/R					
0	0	ac-page			
0	1	gpr: r0-r15			
1	ptr: (r0) to (r15)			off	

ereg	
GPR	
Mem[ptr[0-15]]    ptr[0-15] += offset1/offset2	Always postupdate

This allows access to data memory, ereg and GPR

- Bit 5 = 1: Use rX (X: 0-7) register to obtain effective memory address and post-modify the ptr field by one of two possible offsets specified in rX registers.  
 $dmem[ptr], \text{ ptr} = \text{ptr} + \text{offset1}, \text{ if off} = 0$   
 $\text{ptr} = \text{ptr} + \text{offset2}, \text{ if off} = 1$
- Bit 5 = 0: Access ac-page or GPR

If Bit-4 is set to 0, then bits 3:0 control access to the general-purpose register file (r0-15) or to execution unit registers.

GPR	GPR Intr page	ac-page	ac intr page	ereg-Shadow DSP
R0	R0	A0	A0_i	A0
R1	R1	A1	A1_i	A1
R2	R2	T	T	T
R3	R3	TR	TR	TR
R4	R4			
R5	R5			
R6	R6			
R7	R7			
R8	R8			
R9	R9			SX1
R10	R10			SX1s
R11	R11			SX2
R12	R12_i			SX2s
R13	R13_i			SY1
R14	R14_i			SY1s
R15	R15_i			SY2
				SY2s

FIG. 6C

For shadow DSP instructions, the 3-bit specifier for operands is defined as follows:

2	1	0		2	1	0	
0	0	0	A0	0	0	0	A0
0	0	1	A1	0	0	1	A1
0	1	0	T	0	1	0	T
0	1	1	TR	0	1	1	TR
1	0	0	SX1	1	0	0	SY1
1	0	1	SX1s	1	0	1	SY1s
1	1	0	SX2	1	1	0	SY2
1	1	1	SX2s	1	1	1	SY2s
EREG1				EREG2			

FIG. 6E

Only the shadow DSP instructions can see the above modified page of execution unit registers.

#### 4-bit operand specifier:

Memory operands: (rX) specifies an access out of the data memory to the execution unit for the function that needs to be performed. The address for the access is specified in the rX register in the general register file that hold the 14-bit pointer (16K of addressing) to memory, 5-bit signed offset or a 3-bit unsigned offset that can post-modify the address. In addition each pointer is typed for efficient SIMD processing and includes a permute control for rearranging data elements of a vector on the fly. The "pod" core can deal with 4-element 16-bit real vectors or complex data directly. This ability to manipulate memory data directly reduces the instruction width greatly and allows efficient signal processing.

#### (rX): Memory Address Registers

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
type				cb	x	permute				off1: (0-7)				off0: (-16 to 15)				ptr: pointer													

FIG. 6D

#### 5-bit operand specifier:

The 5-bit specifier includes the 4-bit specifier for general data operands and the special purpose registers. It is used in RISC instructions.

4	3	2	1	0
0	spr: s0-s15			
1	gpr: r0-r15			

SPR		Intr page SPR intr page	
0	fu-ctl	fu-ctl_l	
1	a-type	a-type_l	
2	ps-ctl	ps-ctl	
3	t-type	t-type	
4	pl-ctl	pl-ctl	
5	cb-ctl	cb-ctl_l	
6	shuffle	shuffle	
7	io-ptr	io-ptr	
8	status	status_l	
9	loop-ctl	loop-ctl	
10	pcr	pcr	stack(8)
11	reserved	reserved	
12	reserved	reserved	
13	reserved	reserved	
14	reserved	reserved	

NOTE: All SPR registers are reset to all zeros at power on reset except for the PCR register.

FIG. 6F



DSP Instructions

	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
Multiply	1	0	0	PS	S	SX		SY		V/S	SA	DA		Sub-op						
														0	0	0				Nop
														0	0	1				Add
														0	1	0				Add
														0	1	1				Sub
														1	0	0				Sub
														1	0	1				Min
														1	1	0				Min
														1	1	1				Max
Add	1	0	1	PS	S	SX		SY		V/S	SA	DA		Sub-op						
														0	0	0				Nop
														0	0	1				Add
														0	1	0				AddSub
														0	1	1				Mul
														1	0	0				MuN
														1	0	1				Min
														1	1	0				Max
														1	1	1				CombAdd
Extremum	1	1	0	PS	SX		SY		V/S	SA	DA		Sub-op							
														0	0	0				Nop
														0	0	1				Ext
														0	1	0				Mul
														0	1	1				MuN
														1	0	0				Add
														1	0	1				Sub
														1	1	0				amax
														1	1	1				
type-match	1	1	0	PS	0	SX		SY						1	1	1				
nop	1	1	0	PS	0	1	1	1	1	1	1	1	1	1	1	1				
Permute	1	1	0	PS	1	Type		SY		0	ereg			1	1	1				Permute
Reserved	1	1	1	PS	1	SX		SY		SA	DA	V/S		Sub-op						

Control and specifier Extensions

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mul	0	Pred	PL	Sd	Syt	Prod	LI	S	S	S	S	0	SA	DA	abn	0	0	0	0	0

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Add	0	Pred	PL	Sd	Syt	LI		Sub-ext		0	SA	DA	abn	0	0	0	0	0	0	0
								u	u	u	x									
								x	V/S	Prod	Fp									
								u	u	Gx	Fp									

Nop (unddf)  
 Mu/MuN  
 Min/max

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ext	0	Pred	PL	Sd	Syt	u-cl	Gx	Sub-ext		0	SA	DA	abn	0	0	0	0	0	0	0
								u	Fp											
								Prod	LI											

Add/sub  
 Mul

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	Pred	PL	Pcd2	Syt		Pcd1		0	ereg	Prod	0	0	0	0	0	0	0	0	0

Type/offset/permute extensions

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	Pred	PL	x	Type: SX	Type: SY	0	SA	DA	x	0	1								
	0	Pred	PL	Pos	Permute: SX	Permute: SY	0	SA	DA	Phy	1	0								
	0	Pred	PL	Offset: SX	Offset: SY	0	SA	DA	py	1	1									

Type override  
 permute override  
 Offset override

Shadow DSP

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	Op	PL	op	SA	ereg1	DA	ereg2	1	SA	DA	Sub-op								

nop

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	1	0	PL	0	x	x	x	Prod	x	x	x	0	SA	DA	1	1	1	1	1

FIG. 6H

FIG. 6I

Control Instructions

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
add,sub	L	Pred	0	0	0		RX													
max,min	L	Pred	0	0	0		RX													
Shift	L	Pred	0	0	1		RX													
Logic	L	Pred	0	1	0		RX													
Mux	L	Pred	0	1	1		RX													
mov	L	Pred	0	1	1		RX													
add,zero	L	Pred	0	1	1		RX													
LDm	L	Pred	0	1	1		RX													
Set4bits	L	Pred	1	0	0		U4:POS													
Set2bits	L	Pred	1	0	0		U4:POS													
Setbit	L	Pred	1	0	0		U4:POS													
Movl	L	Pred	1	0	0		U4:POS													
Jmp	L	Pred	1	0	1															
Call	L	Pred	1	0	1															
Loop	L	Pred	1	0	1															
Jmpi	L	Pred	1	0	1															
Calli	L	Pred	1	0	1															
Loopi	L	Pred	1	0	1															
Test	L	Pred	1	1	0															
Testbit	L	Pred	1	1	0															
Andp,orp	L	Pred	1	1	0															
Load	L	Pred	1	1	1															
Store	L	Pred	1	1	1															
eLoad	L	Pred	1	1	1															
eStore	L	Pred	1	1	1															
Extended	L	Pred	1	1	1															
Logic2	L	Pred	1	1	1															
mov-erp	L	Pred	1	1	1															
Car	L	Pred	1	1	1															
Parity	L	Pred	1	1	1															
Stm	L	Pred	1	1	1															
Alu	L	Pred	1	1	1															
Neg	L	Pred	1	1	1															
Div-erp	L	Pred	1	1	1															
Return	L	Pred	1	1	1															
Zero-ac	L	Pred	1	1	1															
eSync	L	Pred	1	1	1															
Swi	L	Pred	1	1	1															
Nop	L	Pred	1	1	1															

\*B41, B43-9-6 = U15 (Shift Amount)

Bit 5: 0-one erreg, 1-broadcast all four; B44: 0=16-bit, 1=32-bit

\*B43, B45-13-10 = U15:POS

FIG. 6J

Extended Control

	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Insert/Extract	RX													
Insert	U4: length	RZ	0	0	0	1	0	2	x	0	RZ	U4: Position		
Shift	RX													
Rotate	RX													
jmp, call	U4: outer LC	U4: inner LC	0	0	1	0	0	Pred	0	R				
doop	RX													
doopi	RX													
mult	RX													
add,sub	RX													
Logic	RX													
Test	RX													
Movl	RX													
load	RX													
store	RX													
loadi	RX													
storei	RX													
Add/subi	RX													
mini/maxi	RX													
and/ori	RX													

FR: Sign/Zero

R = PC relative  
 Bit 15 is continuation of inner LC

andp, orp, andorpc, orandpc: pz = (pz relop py) relop pv)

FIG. 6K

**MAC:**

[illegible]

**ARTM:**

[illegible]

EXT:

[illegible]

**SHIFT:**

35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231	1232	1233	1234	1235	1236	1237	1238	1239	1240	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**Immediate:**

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**Test:**

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**Bunch:**

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37	32	17
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40	29	20
41	28	21
42	27	22
43	26	23
44	25	24
45	24	25
46	23	26
47	22	27
48	21	28
49	20	29
50	19	30
51	18	31
52	17	32
53	16	33
54	15	34
55	14	35
56	13	36
57	12	37
58	11	38
59	10	39
60	9	40
61	8	41
62	7	42
63	6	43
64	5	44
65	4	45
66	3	46
67	2	47
68	1	48
69	0	49
70	0	50

**Wloc;**

FIG. 6L

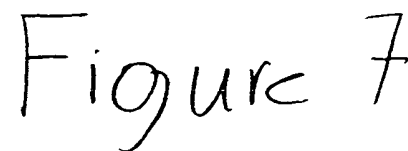


Figure 7

# Pipeline Controller 304

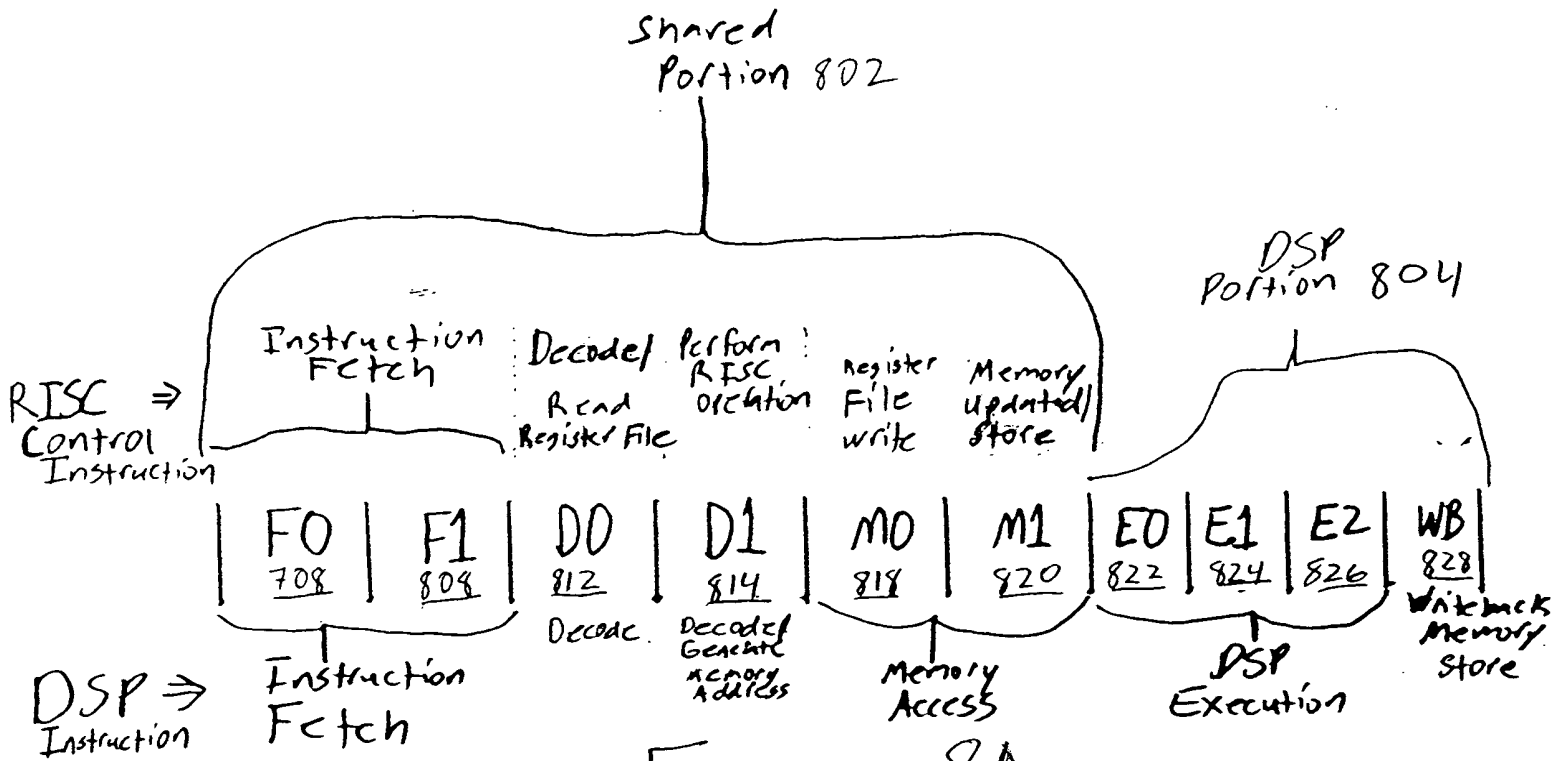


Figure 8A

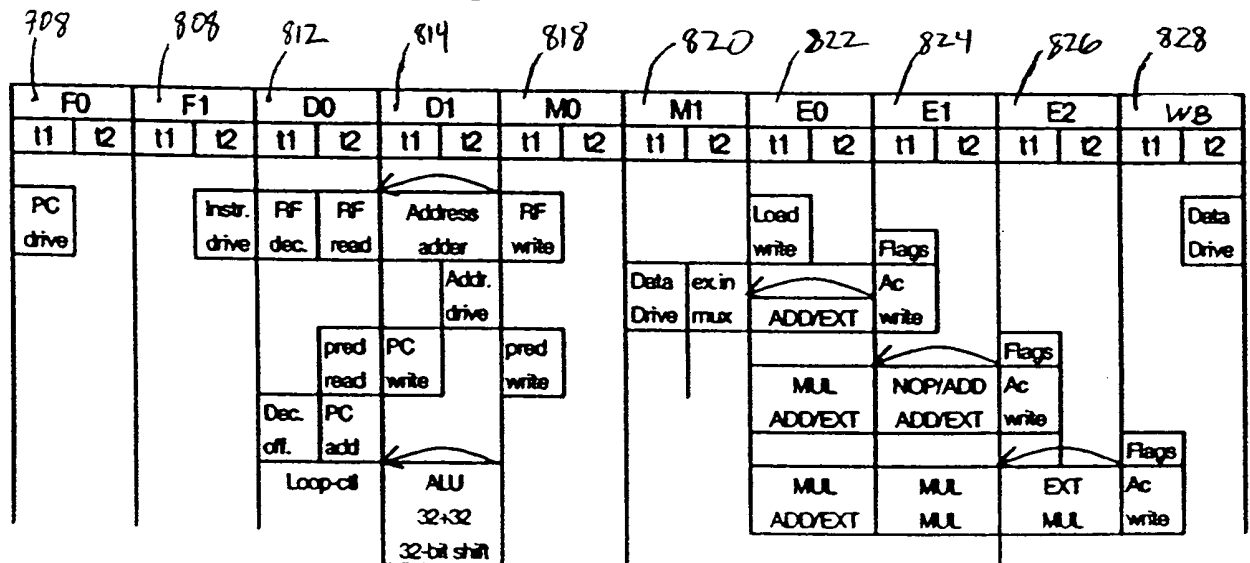


Figure 8B

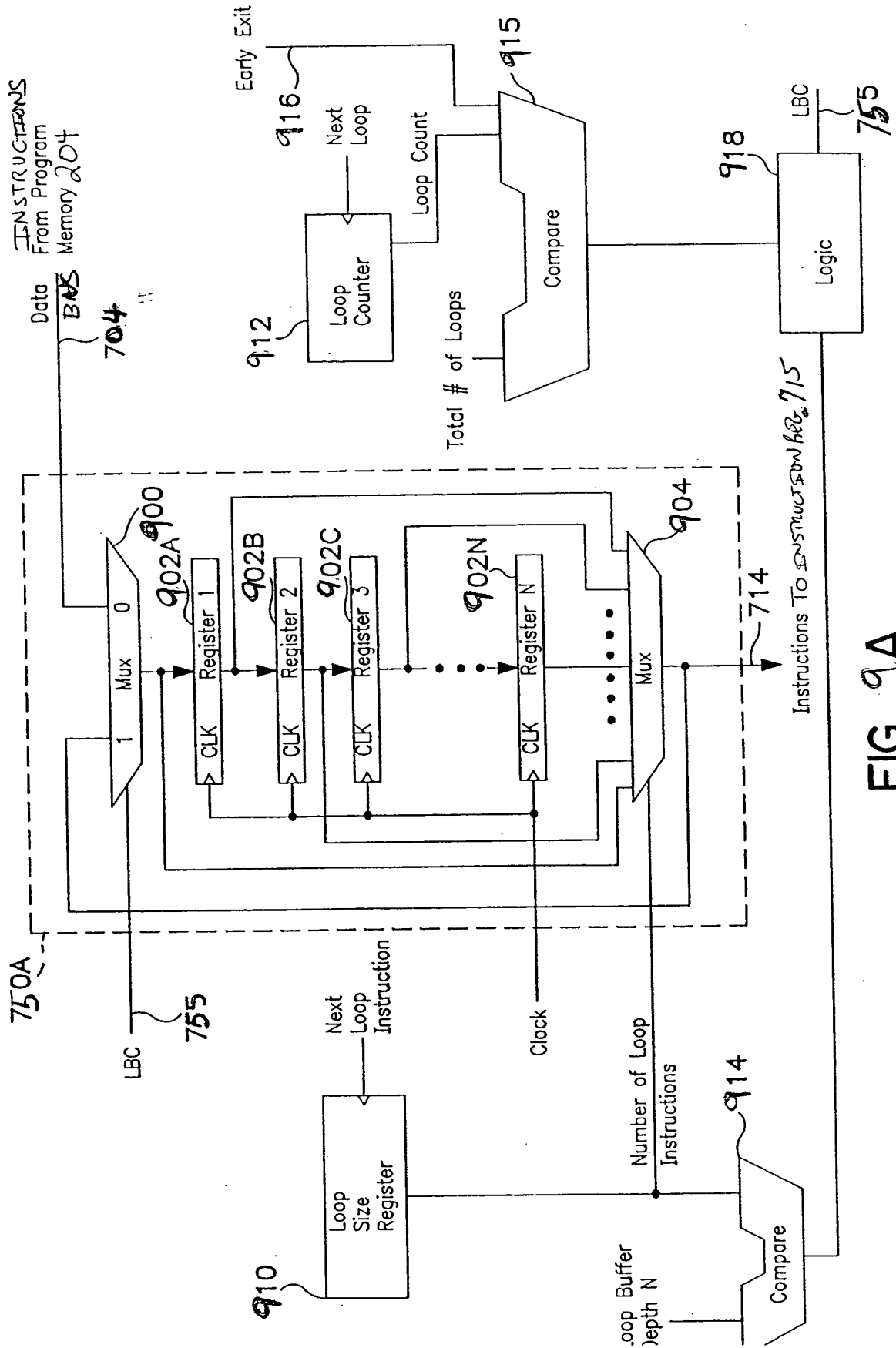
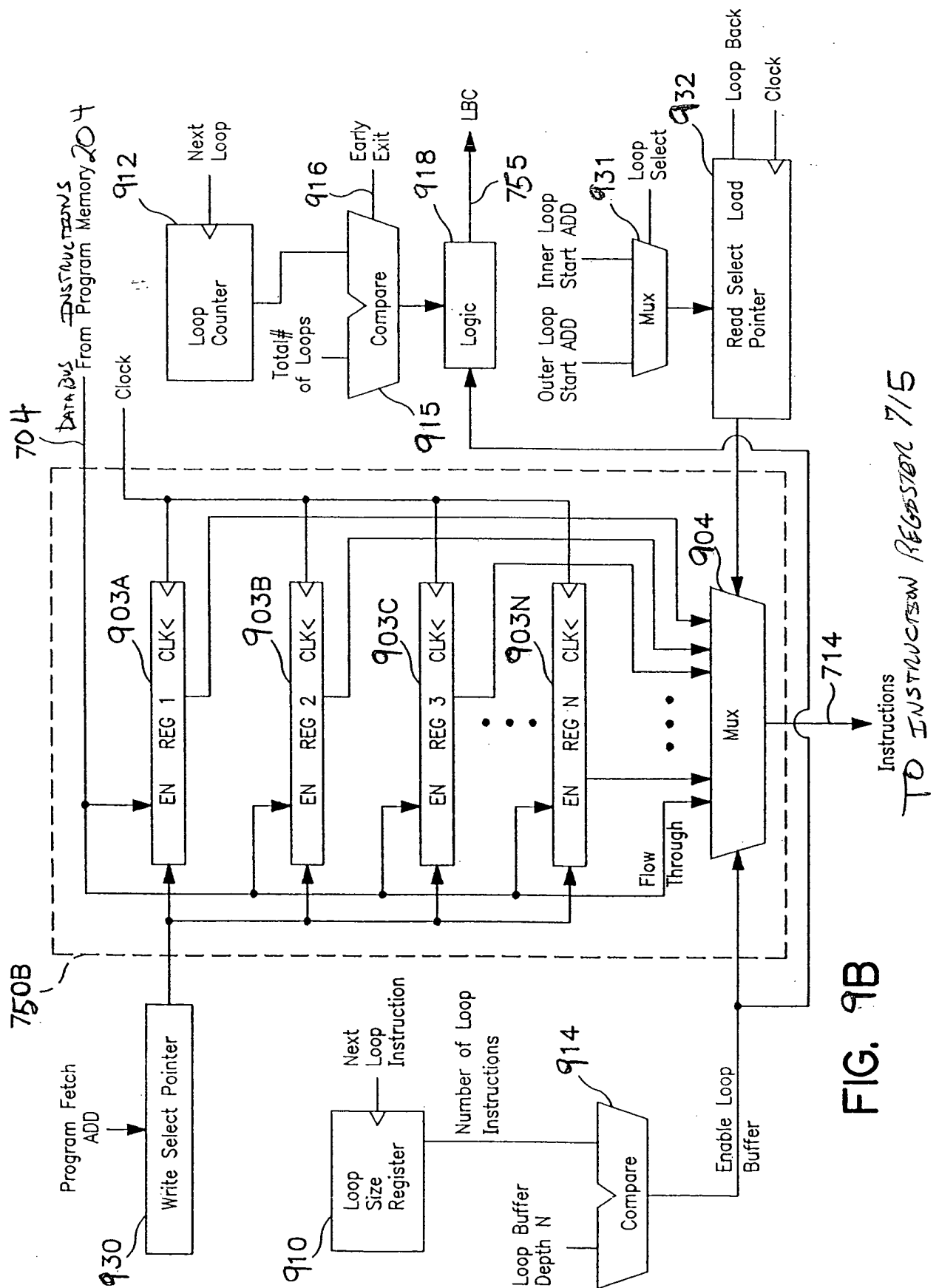


FIG. 9A



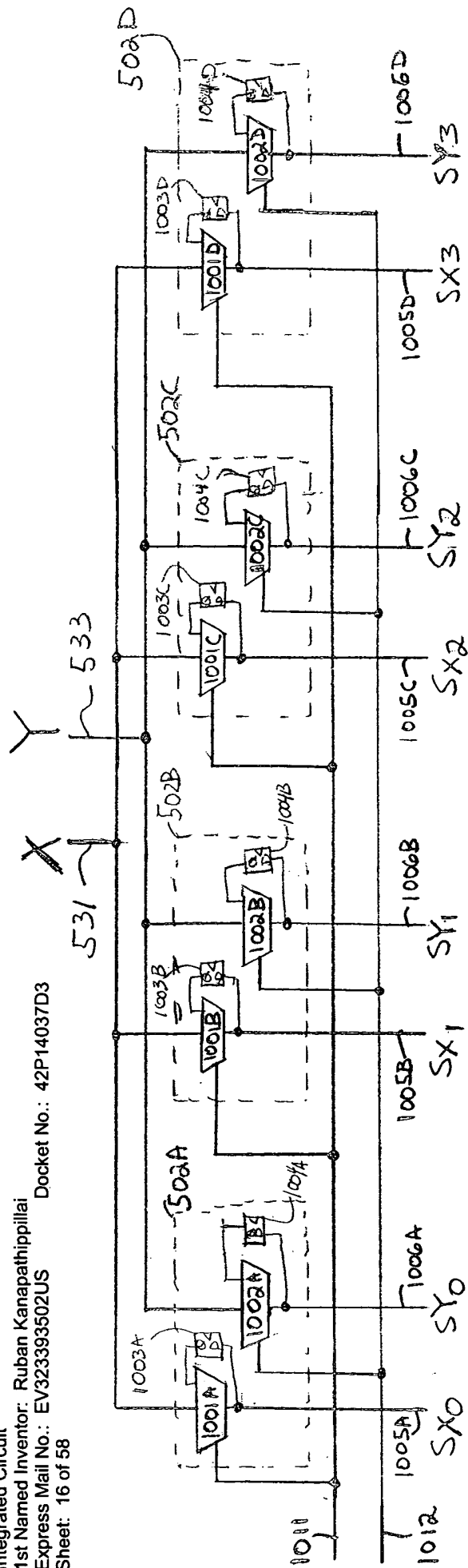


FIG. 10

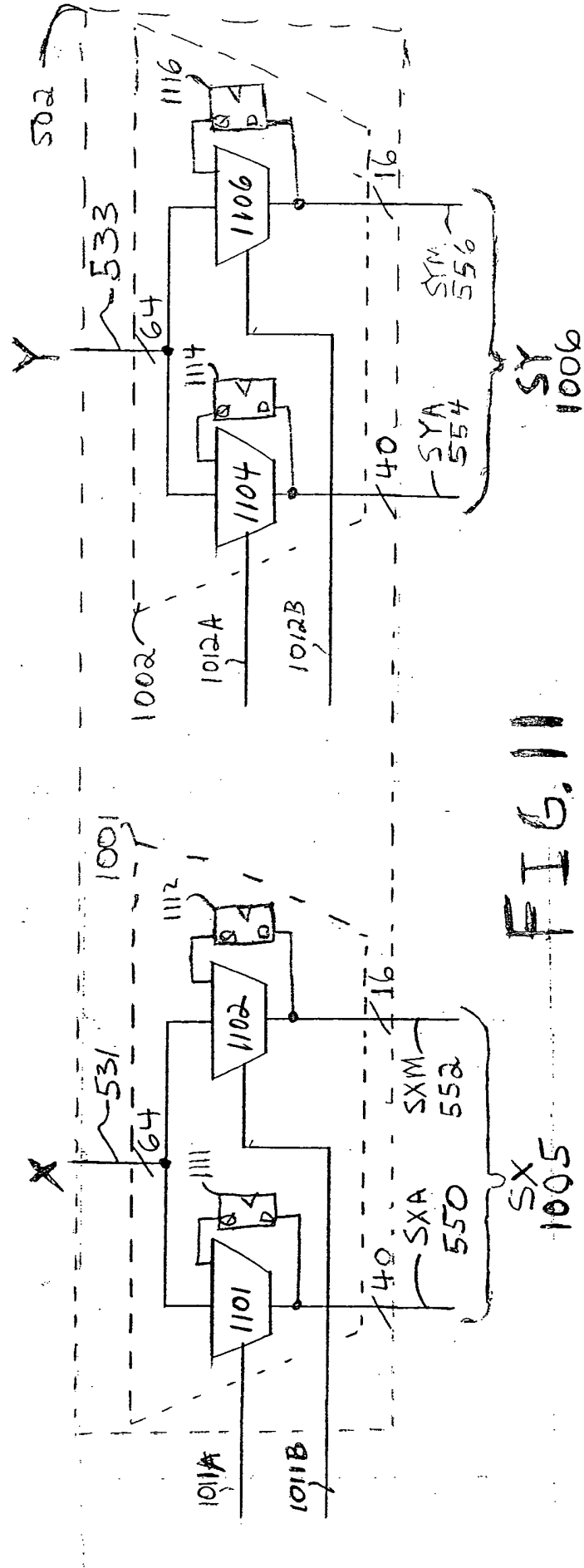


FIG. 11



DATA TYPE

SP CONFIGURATION

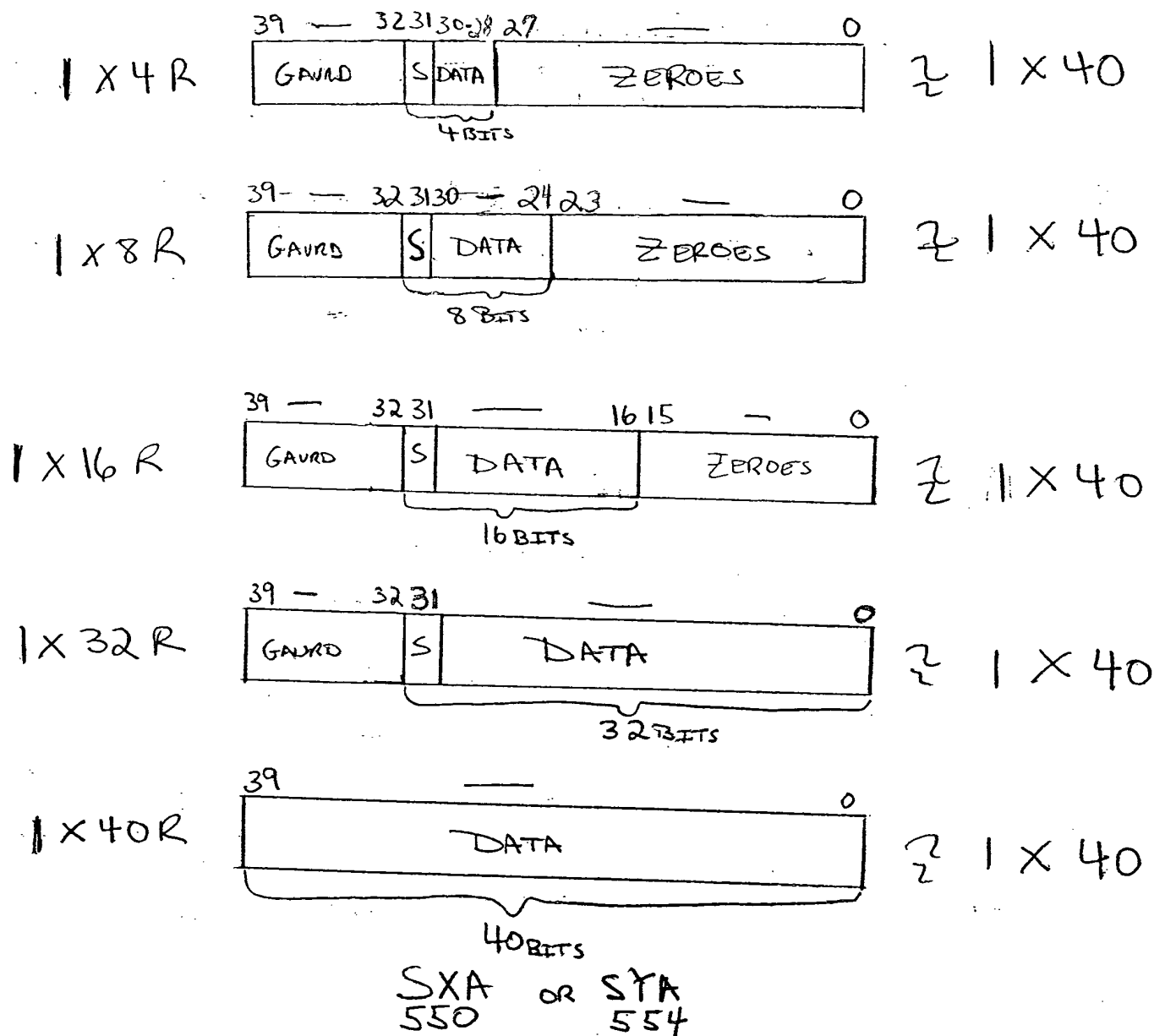
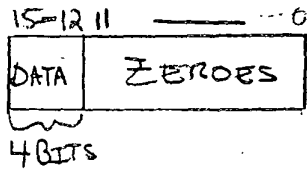


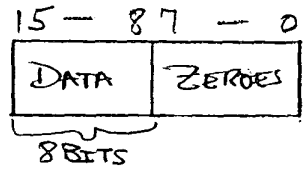
FIG. 12A

# DATA TYPE

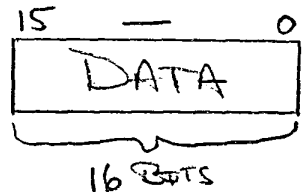
1 x 4 R



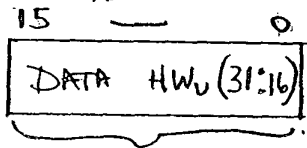
1 x 8 R



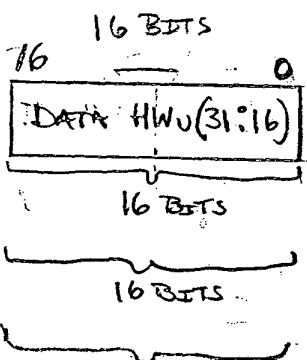
1 x 16 R



1 x 32 R



1 x 40 R



SXM 552A-552B  
OR  
SYM 556A-556B

# SP CONFIGURATION

2 1 x 16

2 1 x 16

2 1 x 16

2 11 x 16

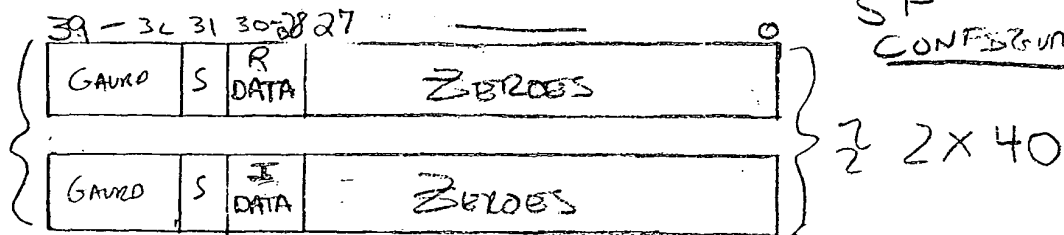
2 11 x 16

FIG. 12B

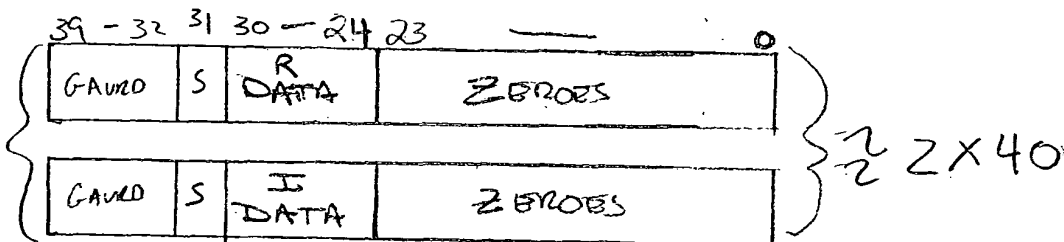
# DATA TYPE

SP  
CONFIGURATION

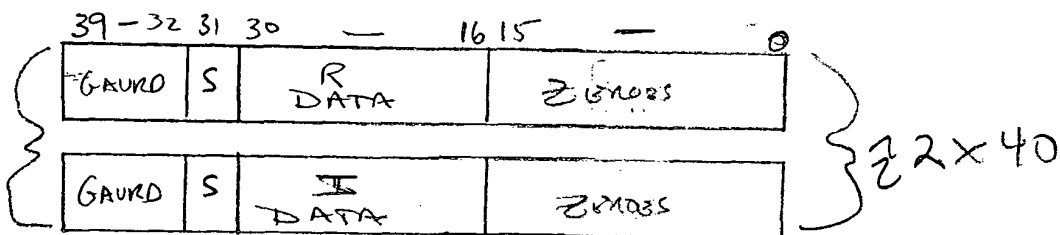
1x4C



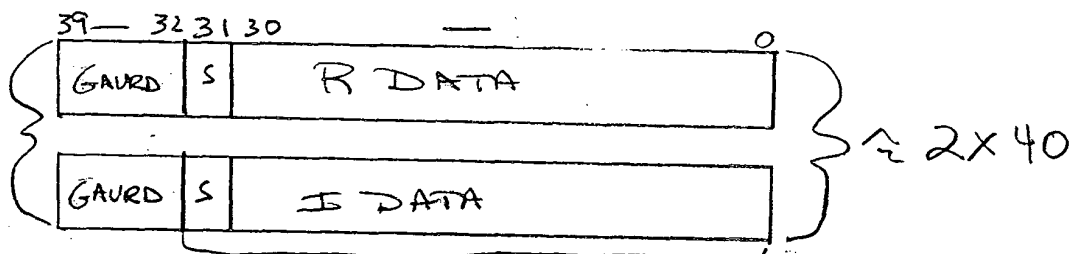
1x8C



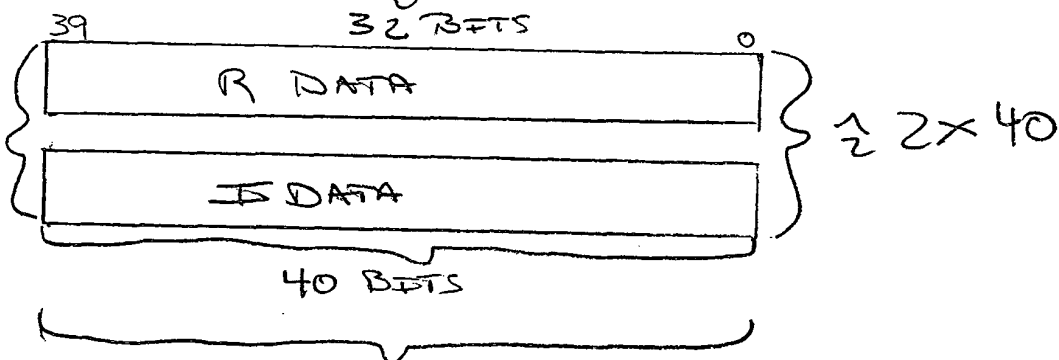
1x16C



1x32C



1x40C

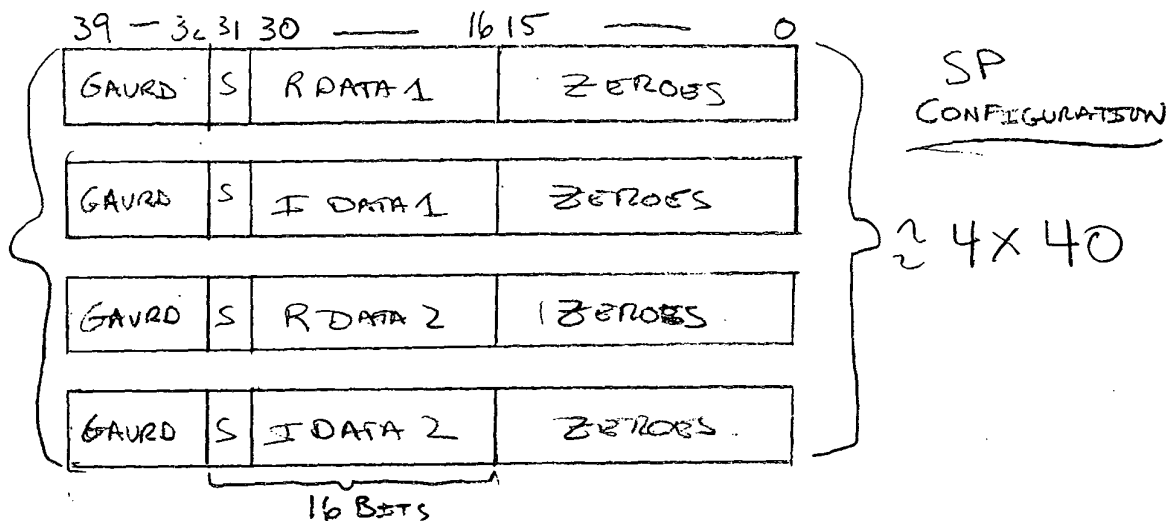


SXA 550A AND SXA 550B  
OR  
SYA 554A AND SYA 554B

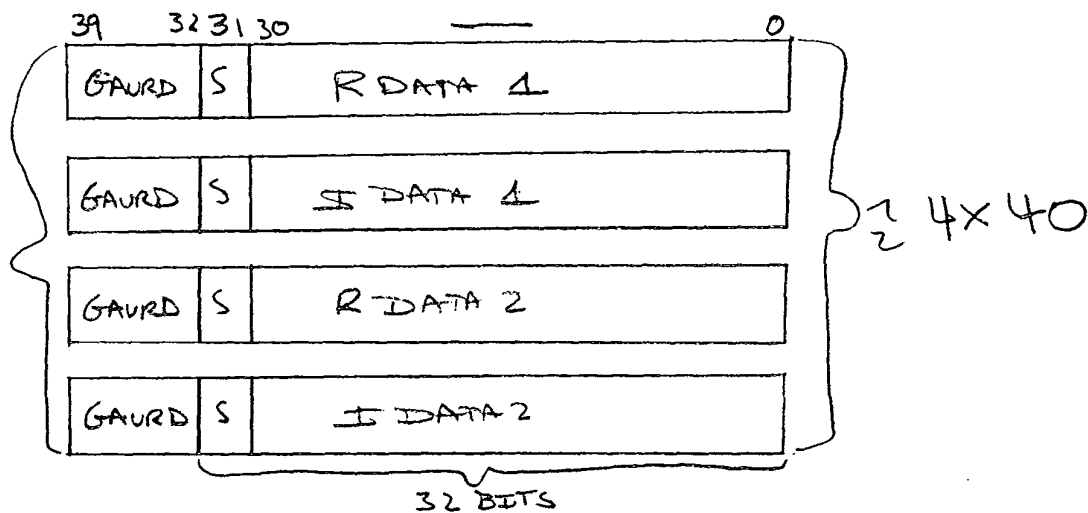
FIG. 12C

DATA TYPE

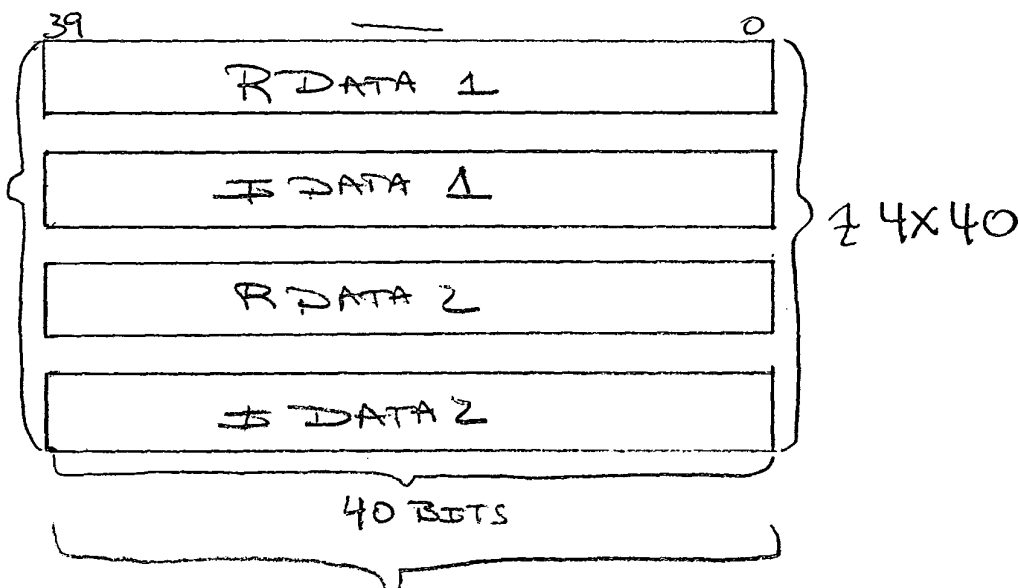
2x16C



2x32C



2x40C



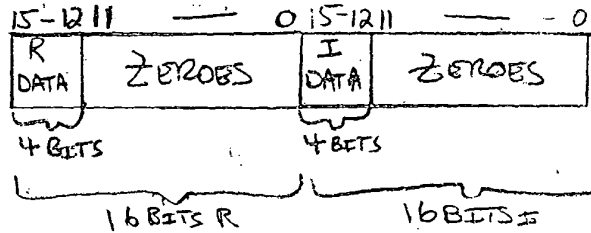
SXA550A, SXA550B, SXA550C, AND SXA550D  
 SYA554A, SYA554B, SYA554C, AND SYA554D

FIG. 12D

# DATA TYPE

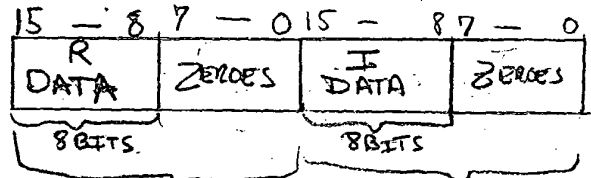
# SP CONFIGURATION

1x4C



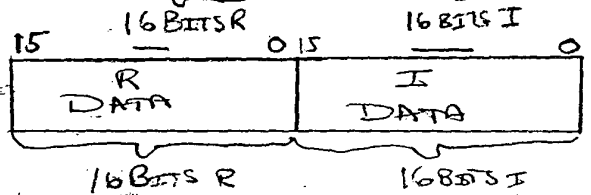
2x16

1x8C



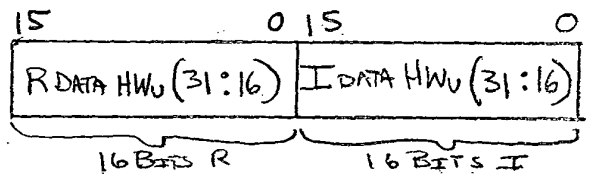
2x16

1x16C



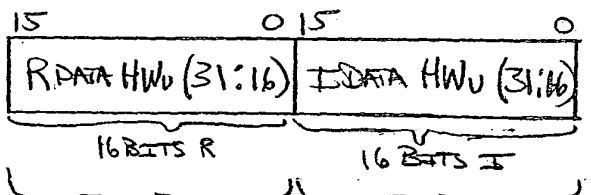
2x16

1x32C



2x16

1x40C



2x16

SXM552A AND SXM552B

OR

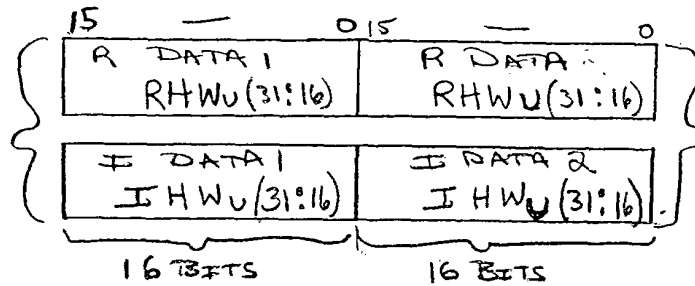
SYM556A AND SYM556B

FIG. 12E

DATA TYPE

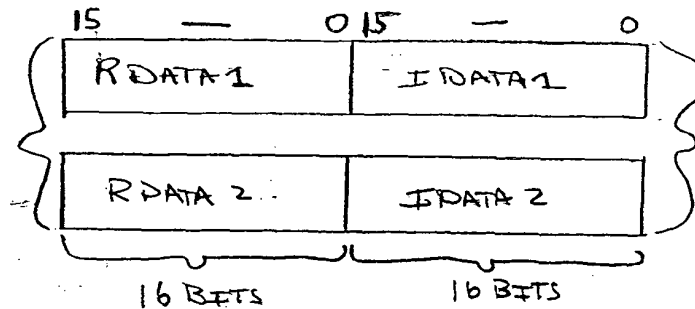
SP CONFIGURATION

2x32C  
OR  
2x40C



2x16

2x16C



2x16

SXM552A, SXM552B, SXM552C, AND SXM552D

SYM556A, SYM556<sup>SR</sup>B, SYM556C, AND SYM556D

FIG. 12F

Operand 1 Data Type:  $N_1 \times S_1 R$   
Operand 2 Data Type:  $N_2 \times S_2 R$   
Type Matching R:  $\text{Max}(N_1 \text{ or } N_2) \times \text{Max}(S_1 \text{ or } S_2) R$

Fig. 13A

Operand 1 Data Type:  $N_1 \times S_1 C$   
Operand 2 Data Type:  $N_2 \times S_2 C$   
Type Matching C:  $\text{Max}(N_1 \text{ or } N_2) \times \text{Max}(S_1 \text{ or } S_2) C$

Fig. 13B

Operand 1 Data Type:  $N_1 \times S_1 R$   
Operand 2 Data Type:  $N_2 \times S_2 C$   
Type Matching R+C:  $\text{Max}(N_1 \text{ or } N_2) \times \text{Max}(S_1 \text{ or } S_2) C$

Fig. 13C

	1x16 real	2x16 real	1x16 cmpx	4x16 real	2x16 cmpx	1x32 real	2x32 real	1x32 cmpx	4x32 real	2x32 cmpx	1x40 real	2x40 real	1x40 cmpx	4x40 real	2x40 cmpx
1x16 real	1 unit	2 unit	2 unit	4 unit	4 unit	2 unit	4 unit	4 unit							
2x16 real	2 unit	2 unit													
1x16 cmpx	2 unit		4 unit												
4x16 real	4 unit			4 unit											
2x16 cmpx	4 unit														
1x32 real	2 unit														
2x32 real	4 unit														
1x32 cmpx	4 unit														
4x32 real															
2x32 cmpx															
1x40 real															
2x40 real															
1x40 cmpx															
4x40 real															
2x40 cmpx															

FIG. 14



	1x16 real	2x16 real	1x16 cmpx	4x16 real	2x16 cmpx	1x32 real	2x32 real	1x32 cmpx	4x32 real	2x32 cmpx	1x40 real	2x40 real	1x40 cmpx	4x40 real	2x40 cmpx
1x16 real	1 unit	2 unit		4 unit		1 unit	4 unit		4 unit		1 unit	2 unit		4 unit	
2x16 real	2 unit	2 unit				2 unit	2 unit					2 unit			
1x16 cmpx															
4x16 real	4 unit			4 unit		4 unit			4 unit					4 unit	
2x16 cmpx															
1x32 real	1 unit	2 unit		4 unit		1 unit	2 unit		4 unit		1 unit	2 unit		4 unit	
2x32 real	4 unit	2 unit				2 unit	2 unit					2 unit			
1x32 cmpx															
4x32 real	4 unit			4 unit		4 unit			4 unit		4 unit			4 unit	
2x32 cmpx															
1x40 real	1 unit					1 unit			4 unit		1 unit				
2x40 real	2 unit	2 unit				2 unit	2 unit					2 unit			
1x40 cmpx															
4x40 real	4 unit		4 unit			4 unit			4 unit					4 unit	
2x40 cmpx															

FIG. 15A

	1x16 real	2x16 real	1x16 cmpx	4x16 real	2x16 cmpx	1x32 real	2x32 real	1x32 cmpx	4x32 real	2x32 cmpx	1x40 real	2x40 real	1x40 cmpx	4x40 real	2x40 cmpx
1x16 real	1 unit	2 unit	2 unit	4 unit	4 unit	1 unit	2 unit	2 unit	4 unit	4 unit	1 unit	2 unit	2 unit	4 unit	4 unit
2x16 real	2 unit	2 unit				2 unit	2 unit					2 unit			
1x16 cmpx	2 unit		2 unit					2 unit			2 unit		2 unit		
4x16 real	4 unit			1 unit		4 unit			4 unit					4 unit	
2x16 cmpx	4 unit				4 unit					4 unit					4 unit
1x32 real	1 unit	2 unit				1 unit	2 unit	2 unit	4 unit		1 unit	2 unit	2 unit	4 unit	
2x32 real	2 unit	2 unit				2 unit	2 unit					2 unit			
1x32 cmpx	2 unit		2 unit			2 unit		2 unit			2 unit		2 unit		
4x32 real	4 unit			4 unit		4 unit			4 unit		4 unit			4 unit	
2x32 cmpx	4 unit				4 unit					4 unit					4 unit
1x40 real	1 unit		2 unit			1 unit		2 unit	4 unit		1 unit	2 unit		4 unit	
2x40 real	2 unit	2 unit				2 unit	2 unit				2 unit	2 unit			
1x40 cmpx	2 unit		2 unit			2 unit		2 unit					2 unit		
4x40 real	4 unit			4 unit		4 unit			4 unit		4 unit			4 unit	
2x40 cmpx	4 unit				4 unit					4 unit					4 unit

FIG. 15 B

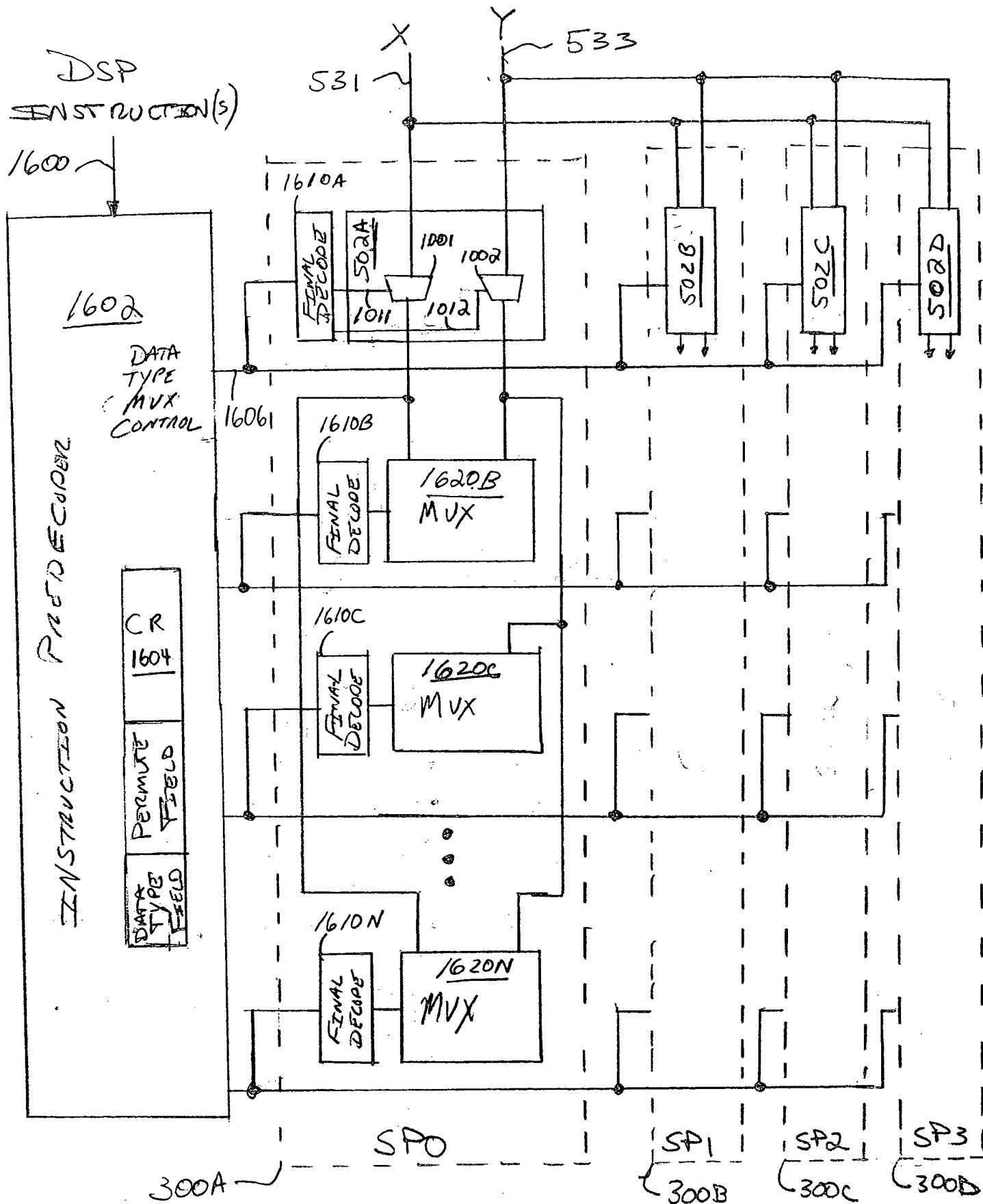


FIG. 16

Data Type:  $N \times S(R/C)$

FIG. 17

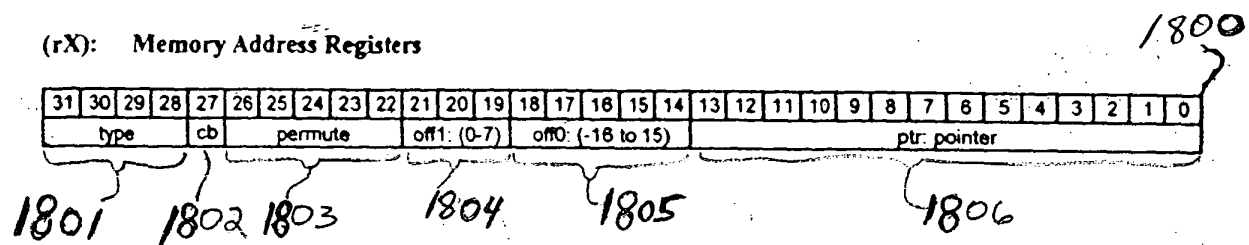


FIG. 18

DATA TYPE 1801

- 0000: 1x16 real
- 0001: 2x16 real
- 0010: 1x16 complex
- 0011: 4x16 real
- 0100: 1x32 real
- 0101: 2x32 real
- 0110: 1x32 complex
- 0111: 2x16 complex
- 1000: 4x32 real
- 1001: 2x32 complex
- 1010: 1x40 real
- 1011: 2x40 real
- 1100: 1x40 complex
- 1101: 4x40 real (only for local add unit operations)
- 1110: 2x40 complex (only for local add unit operations)
- 1111: Reserved

FIG. 19

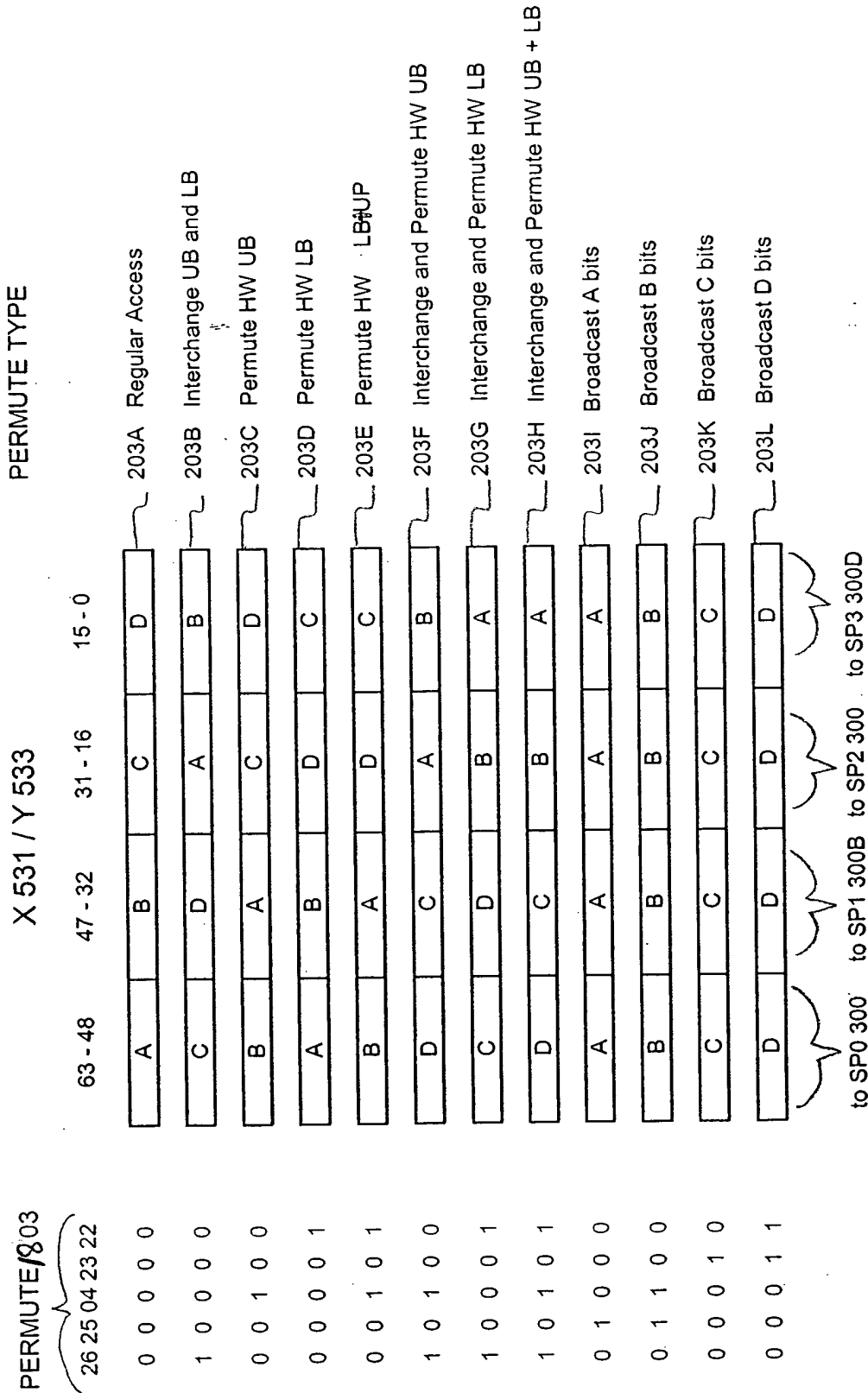


FIG. 20

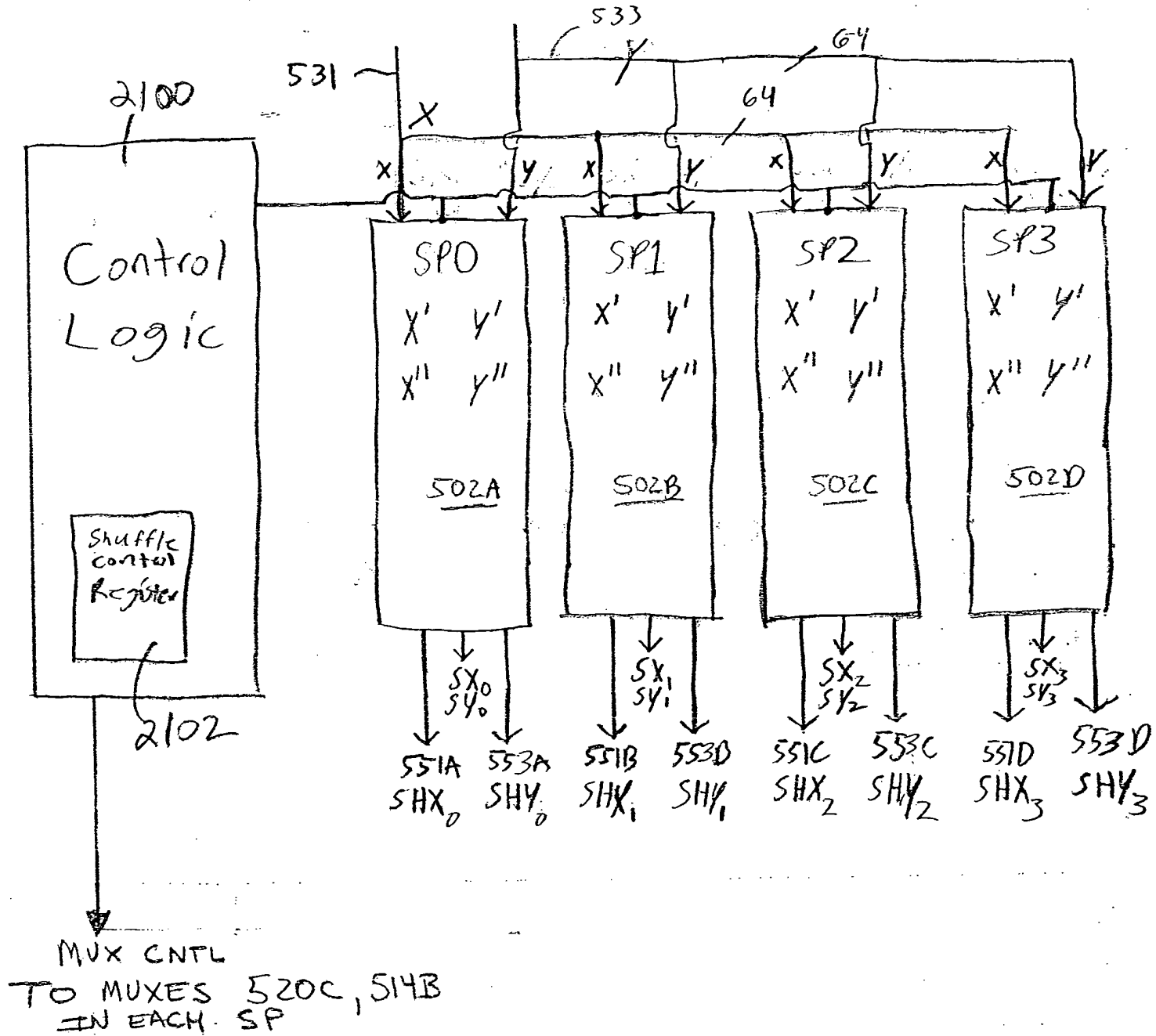


FIG. 21

$$X' = [SX_{10}, SX_{11}, SX_{12}, SX_{13}] \text{ e.g. } [x_0, x_1, x_2, x_3]$$

$$X'' = [SX_{20}, SX_{21}, SX_{22}, SX_{23}] \text{ e.g. } [x_4, x_5, x_6, x_7]$$

Where  $SX_{ab}$ : S=Source; a=delay; b= SP unit number (e.g. SP3, SP1, SP0; or termed  $u_3, u_2, u_1, u_0$ )

$$y' = [SY_{10}, SY_{11}, SY_{12}, SY_{13}]$$

$$y'' = [SY_{20}, SY_{21}, SY_{22}, SY_{23}]$$

Where  $SY_{ab}$ : S=Source; a=delay; b= SP unit number (e.g. SP3, SP2, SP1, SP0; or termed  $u_3, u_2, u_1, u_0$ )

FIG. 22A

shuffle

Shuffle Control Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
u3	u2	u1	u0	u3	u2	u1	u0	u3	u2	u1	u0	u3	u2	u1	u0	u3	u2	u1	u0	u3	u2	u1	u0	u3	u2	u1	u0	u3	u2	u1	u0
SY2S								SY1S								SX2S								SX1S							

Units are connected to their nearest neighbors for shuffling the sources using the following bit diagram:

- 00 Unit N+1, SX1 =  $X'$  (right)
- 01 Unit N+1, SX2 =  $X''$  (right)
- 10 Unit N-1, SX1 =  $X'$  (left)
- 11 Unit N-1, SX2 =  $X''$  (left)

For example to shift the sources to the left by one:

3	2	1	0	From
2	1	0	3	Into

The bits should be 10101010 (\$AA)

FIG. 22C

FIR Filter  $\begin{bmatrix} x_0 \\ x_1 \\ \vdots \\ x_N \end{bmatrix} * \begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix} = x_0 y_0 + x_1 y_1 + \dots + x_N y_N$

### Primary Stage

Cycle #

1

2

3

⋮

N

### Primary Stage Computations

SP0

SP1

SP2

SP3

$$x_0 y_0 + \boxed{x_1} y_1 + \boxed{x_2} y_2 + \boxed{x_3} y_3$$

$$\boxed{x_4} y_4 + \boxed{x_5} y_5 + \boxed{x_6} y_6 + \boxed{x_7} y_7$$

$$\boxed{x_8} y_8 + x_9 y_9 + x_{10} y_{10} + x_{11} y_{11}$$

$$\vdots$$

$$x_{N-3} y_{N-3} + x_{N-2} y_{N-2} + x_{N-1} y_{N-1} + x_N y_N$$

### Shadow Stage

Cycle #

1

No operation

2

No operation

3

4

⋮

N+2

### Shadow Stage Computations

SP0

SP1

SP2

SP3

$$\boxed{x_1} y_0 + \boxed{x_2} y_1 + \boxed{x_3} y_2 + \boxed{x_4} y_3$$

$$\boxed{x_5} y_4 + \boxed{x_6} y_5 + \boxed{x_7} y_6 + \boxed{x_8} y_7$$

$$\vdots$$

$$x_{N-2} y_{N-3} + x_{N-1} y_{N-2} + x_N y_{N-1} + x_{N+1} y_N$$

$$\begin{bmatrix} x_1 \\ \vdots \\ x_{N+1} \end{bmatrix} * \begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix}$$

(Shuffle  $x'$  Left by one)

### Subsequent Cycles

#### Primary Stage

Cycle #

N+1

⋮

2N

⋮

N+4

⋮

3N

$$\begin{bmatrix} x_2 \\ \vdots \\ x_{N+2} \end{bmatrix}$$

\*

$$\begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix}$$

#### Shadow Stage

Cycle #

N+3

⋮

N+5

⋮

N+5

⋮

N+7

$$\begin{bmatrix} x_3 \\ \vdots \\ x_{N+3} \end{bmatrix}$$

\*

$$\begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix}$$

$$\begin{bmatrix} x_4 \\ \vdots \\ x_{N+4} \end{bmatrix}$$

\*

$$\begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix}$$

$$\begin{bmatrix} x_5 \\ \vdots \\ x_{N+5} \end{bmatrix}$$

\*

$$\begin{bmatrix} y_0 \\ \vdots \\ y_N \end{bmatrix}$$

⋮

FIG. 22B



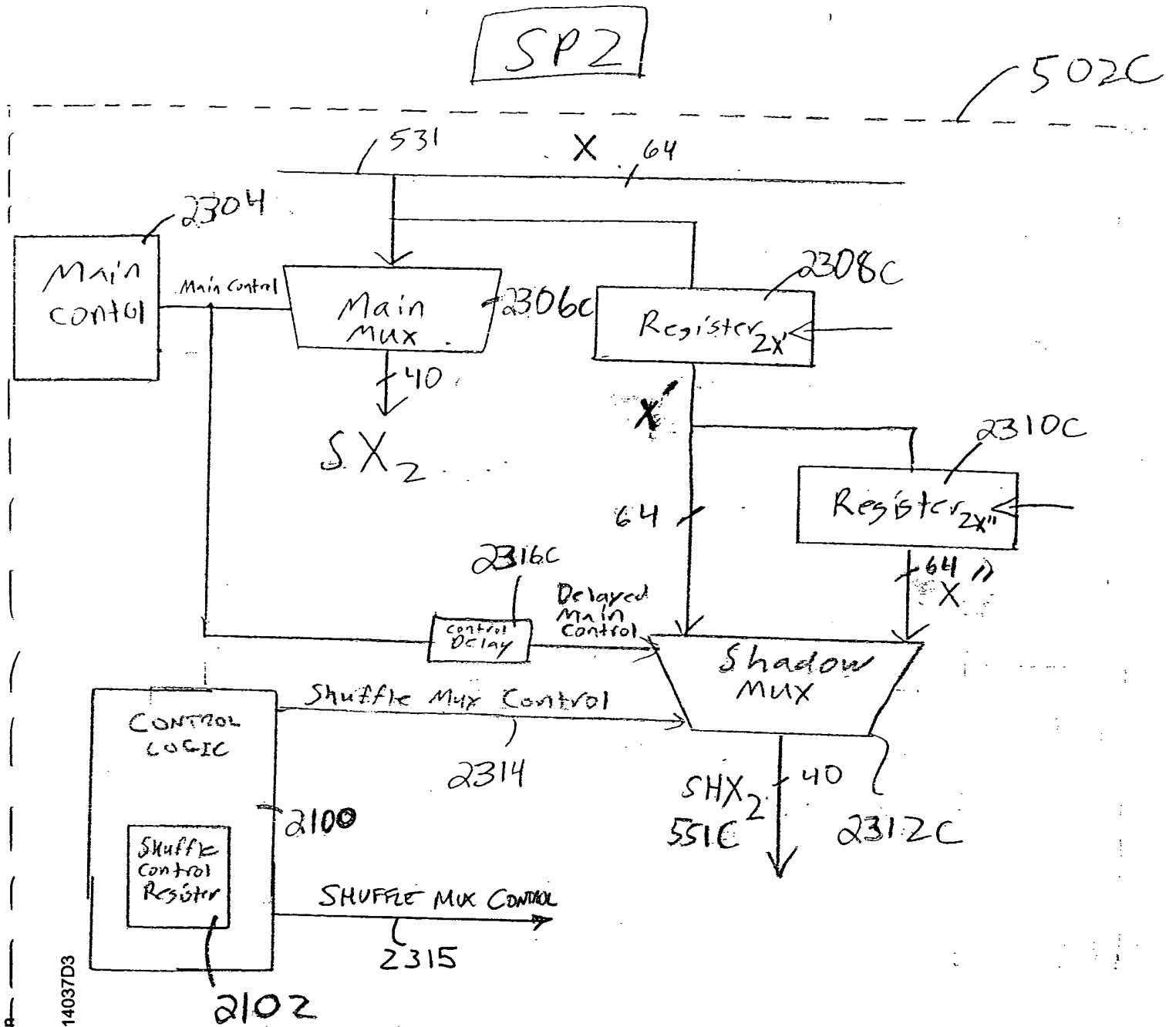


FIG. 23A

FIG. 23A

FIG. 23B

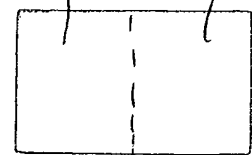
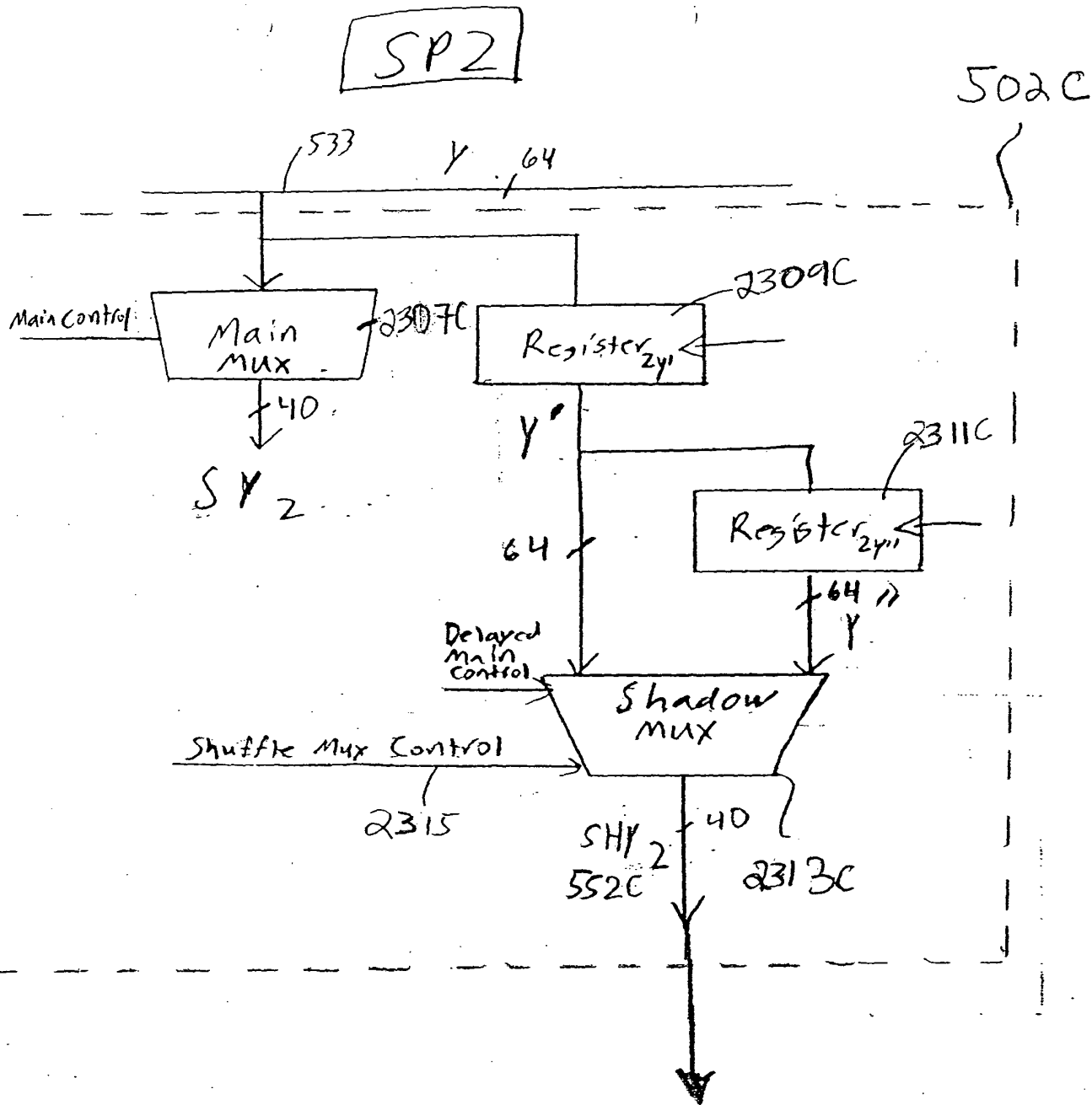


FIG. 23



**FIG. 23B**

Blakely, Sokoloff, Taylor & Zafman LLP  
 Title: Memory with Memory Clusters for Power Reduction in an  
 Integrated Circuit  
 1st Named Inventor: Ruban Kanapathippillai  
 Express Mail No.: EV323393502US  
 Sheet: 35 of 58  
 (714) 557-3800  
 Docket No.: 42P14037D3

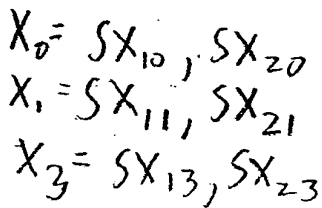
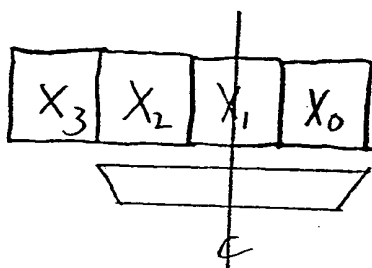
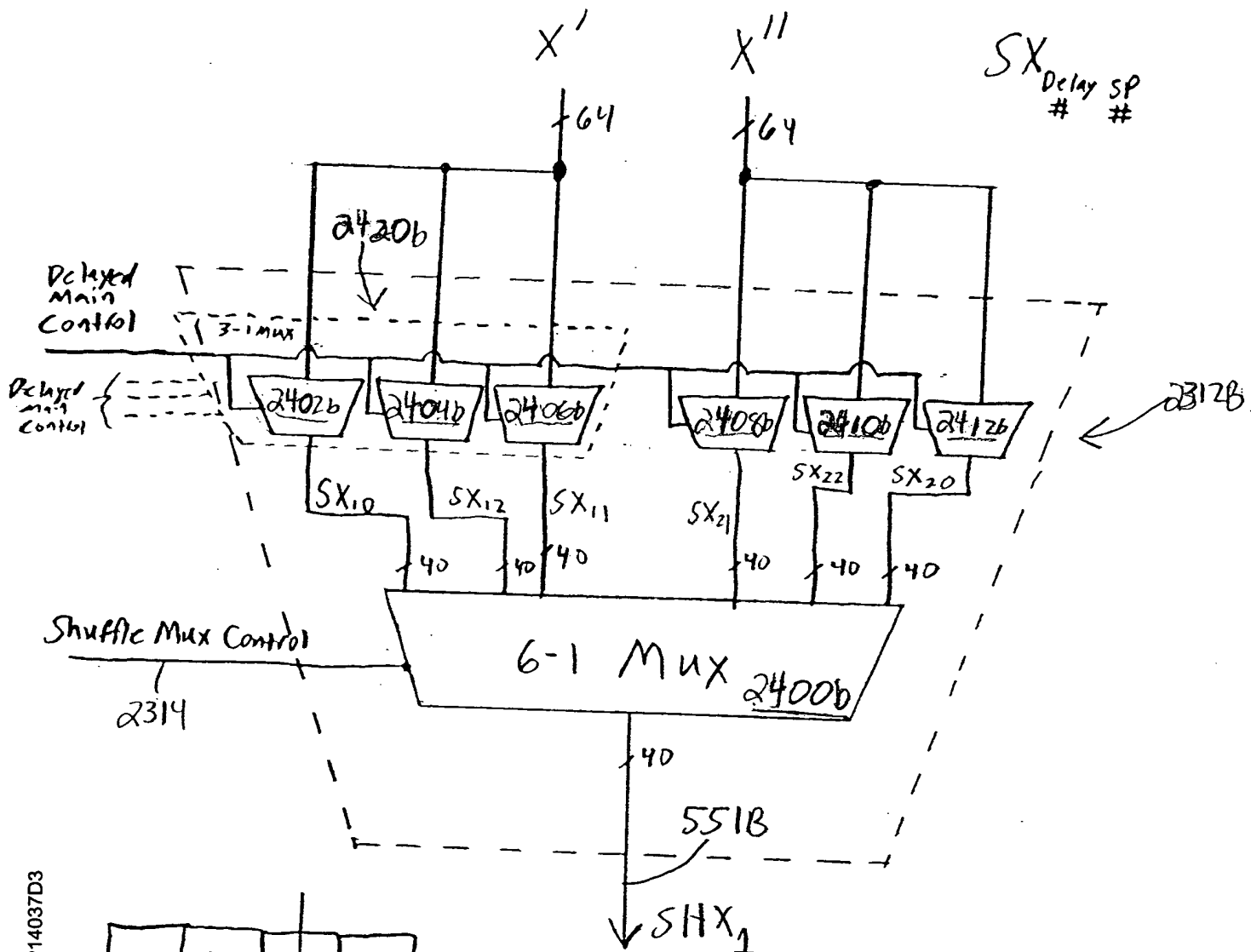


FIG. 24A

# SP1 Shadow Mux



$$\begin{aligned} X_1 &= SX_{11}, SX_{21} \\ X_2 &= SX_{12}, SX_{22} \\ X_0 &= SX_{10}, SX_{20} \end{aligned}$$

FIG. 24B

# SP2 Shadow Mux

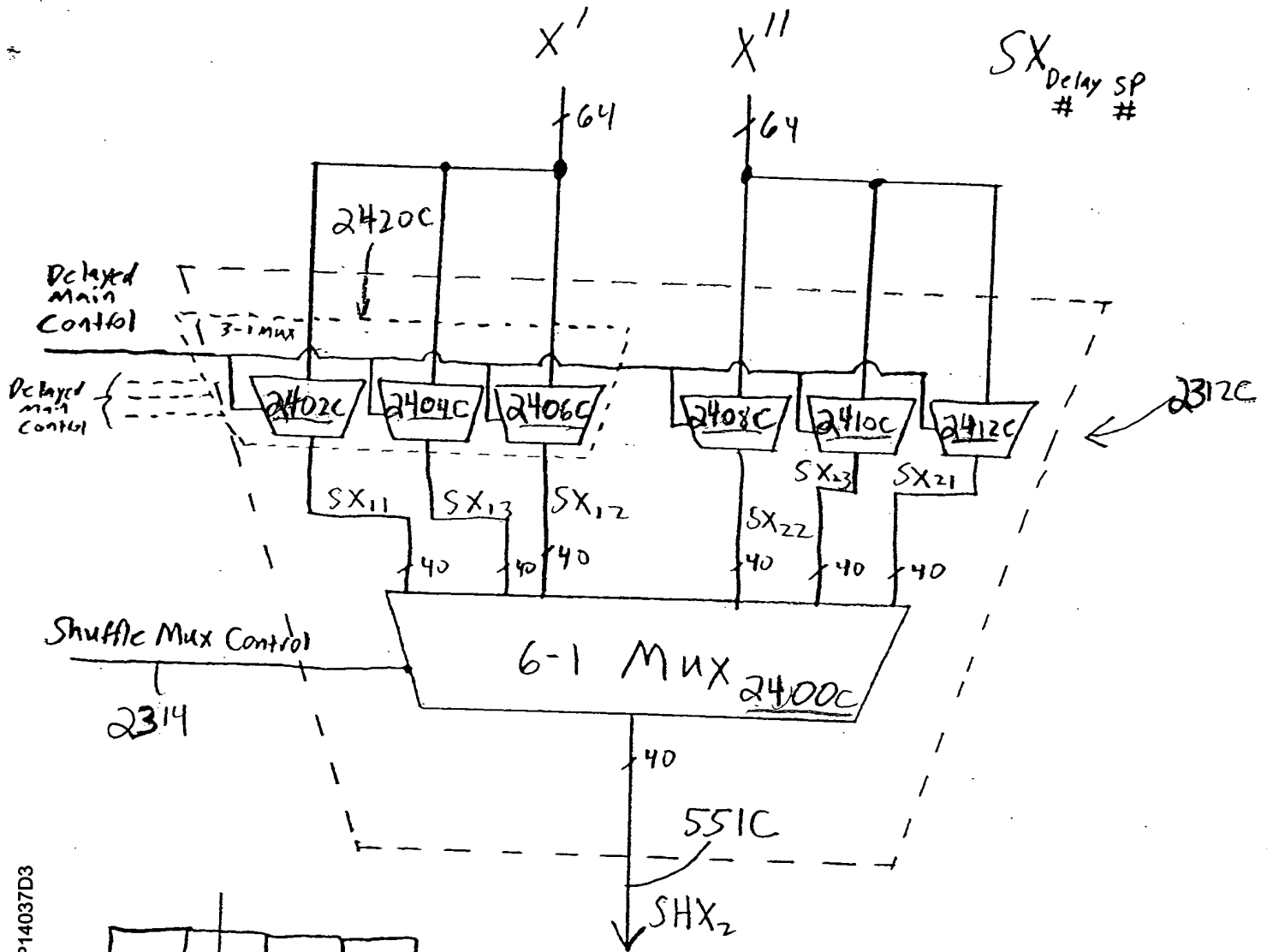


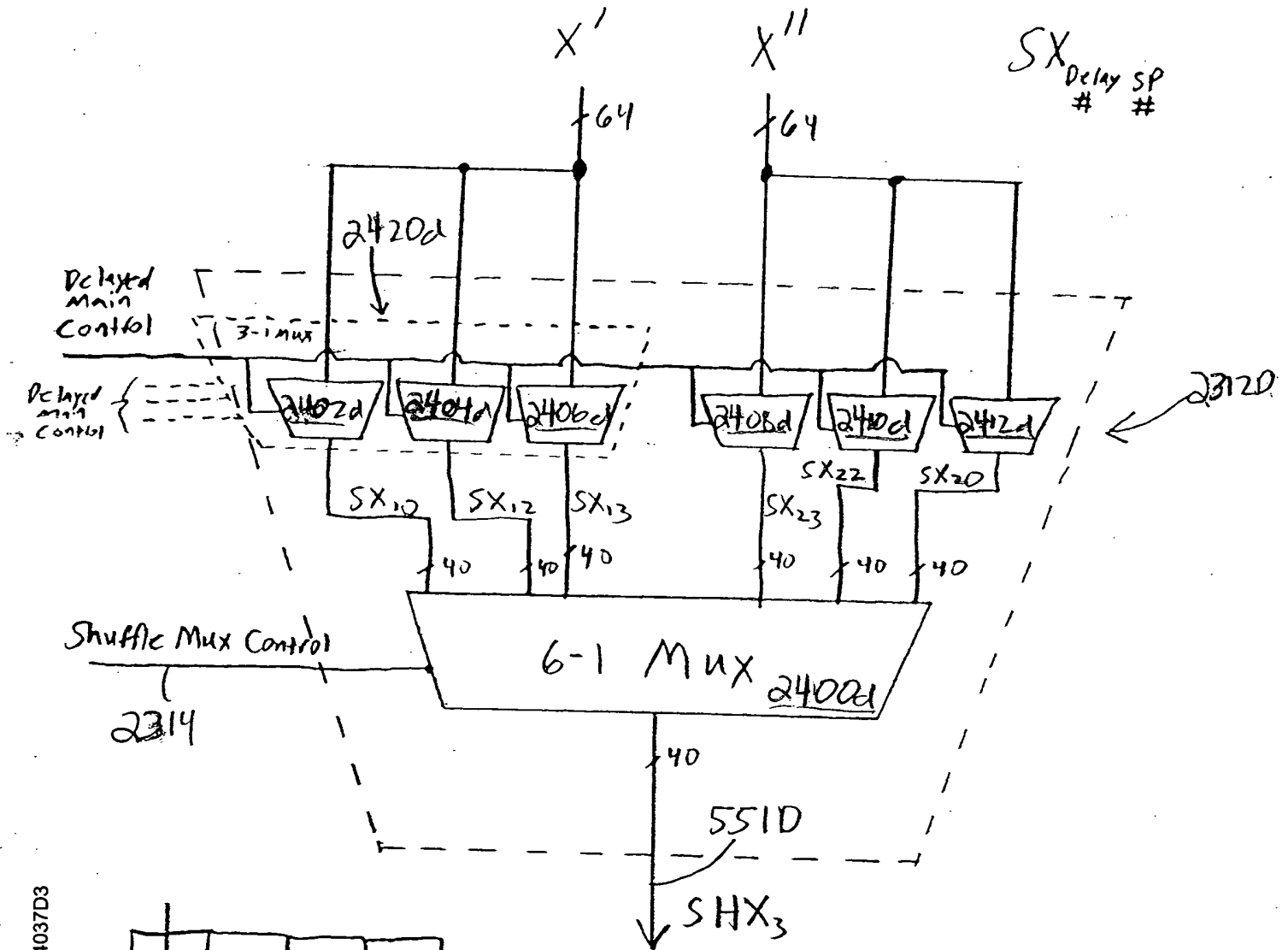
FIG. 24C

$$X_2 = SX_{12}, SX_{22}$$

$$X_3 = SX_{13}, SX_{23}$$

$$X_1 = SX_{11}, SX_{21}$$

# SP3 Shadow Mux



$$\begin{aligned} X_3 &= SX_{13}, SX_{23} \\ X_0 &= SX_{10}, SX_{20} \\ X_2 &= SX_{12}, SX_{22} \end{aligned}$$

FIG. 24D

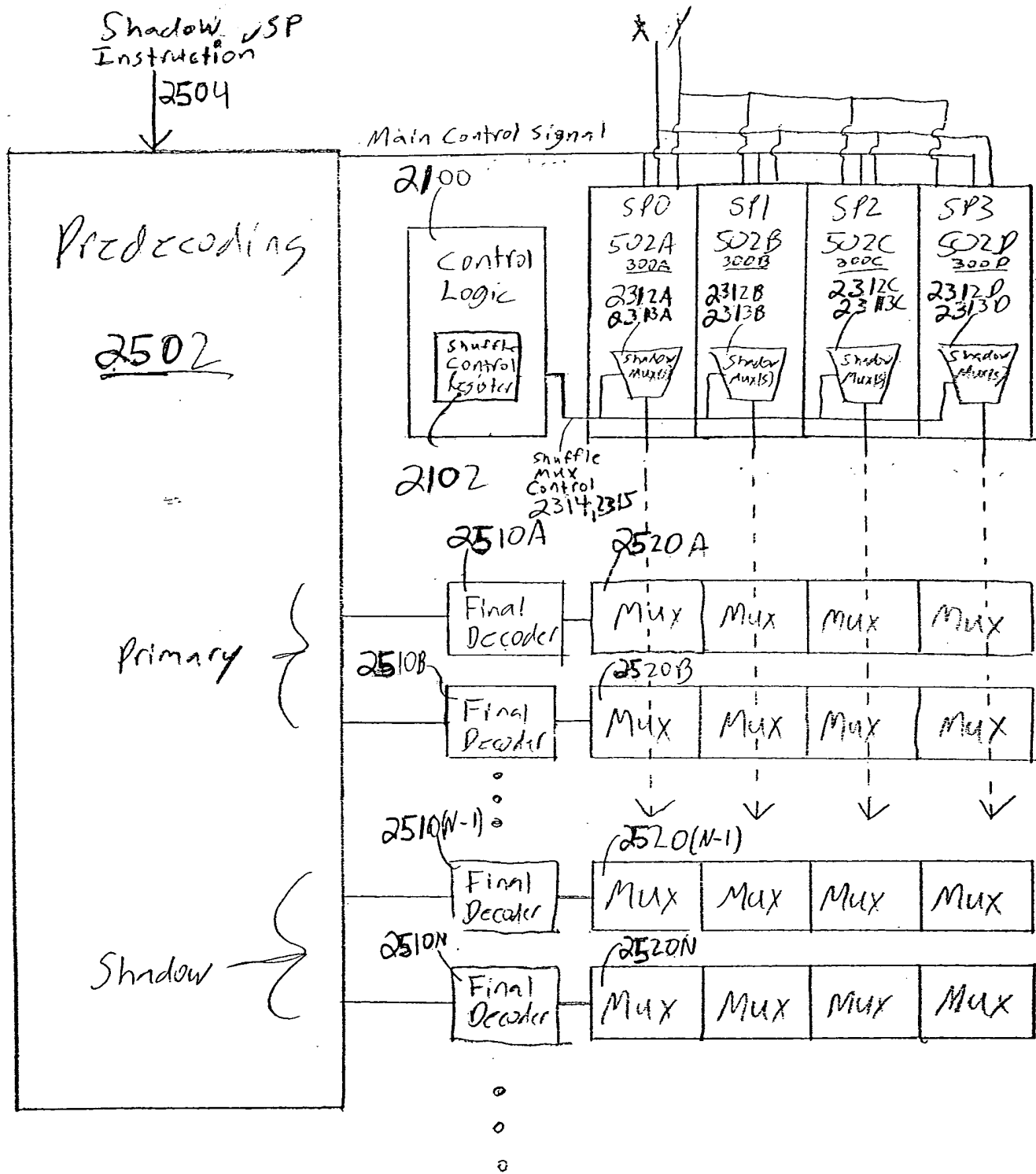


FIG. 25

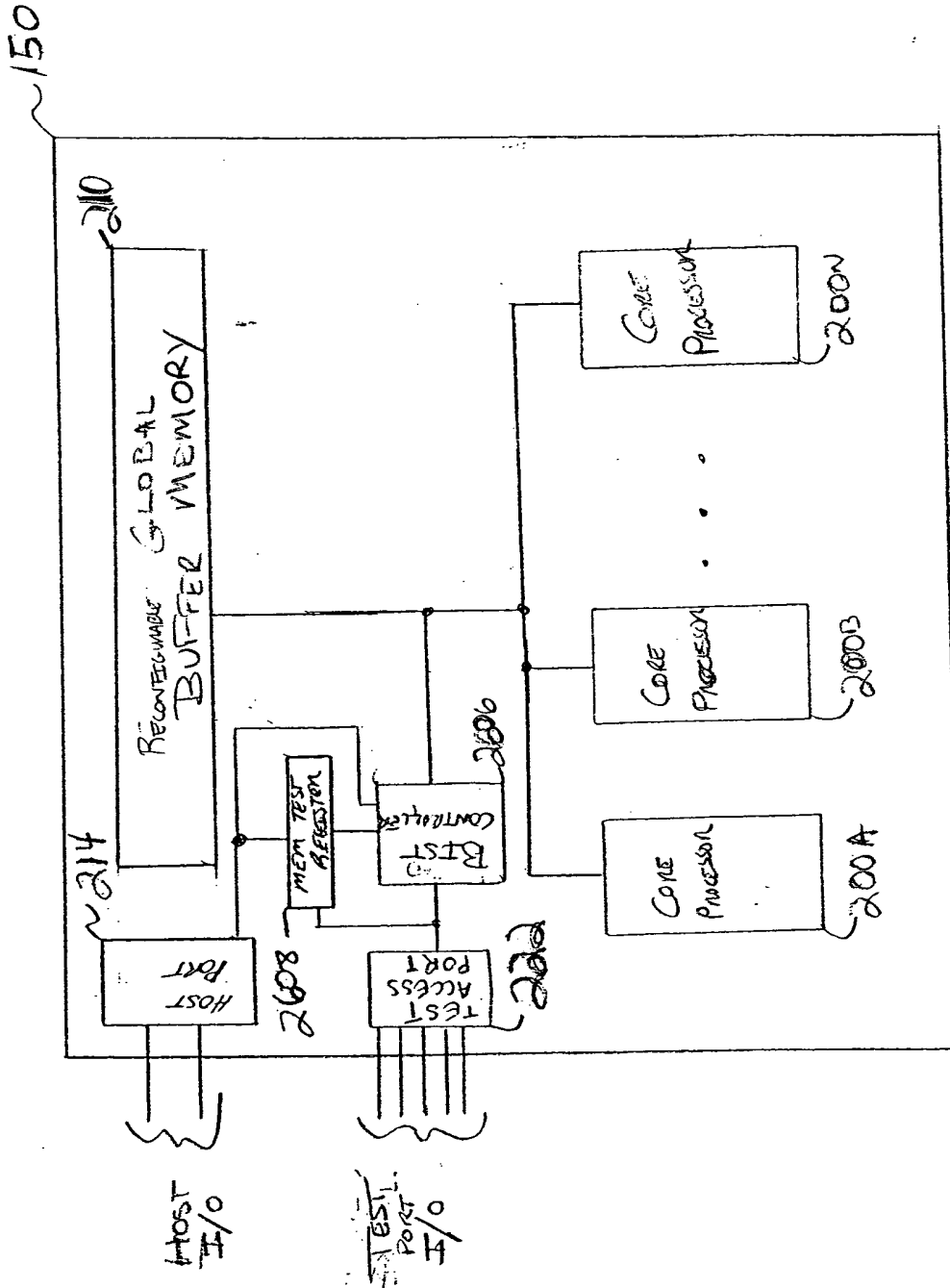
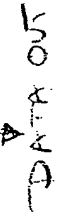


FIG. 26





Address

 $\alpha/3$

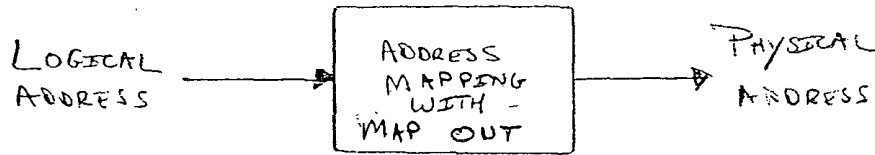
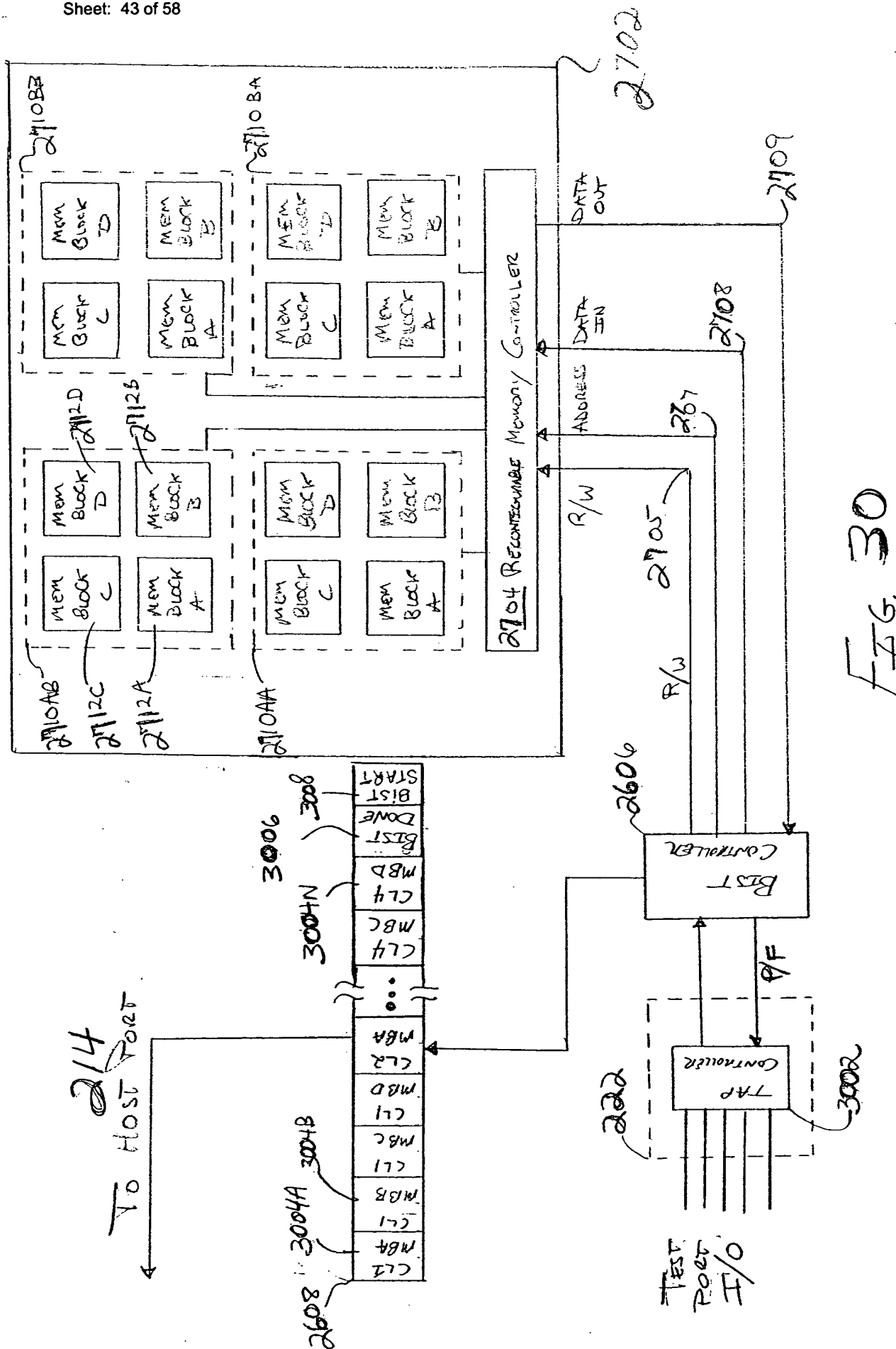
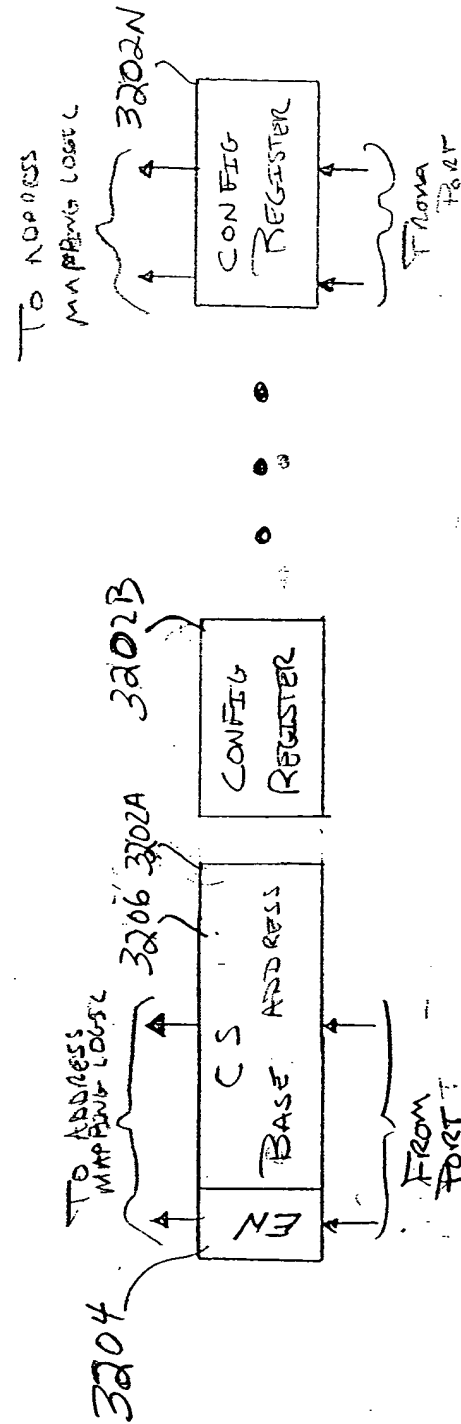
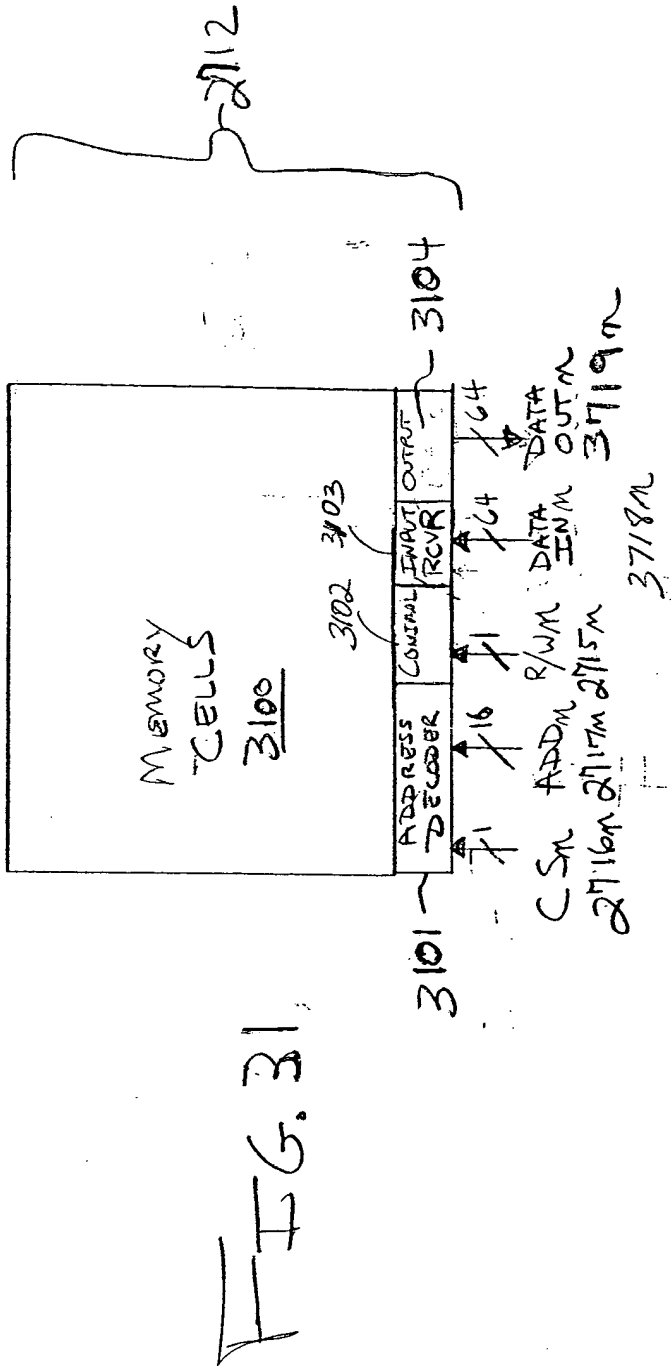


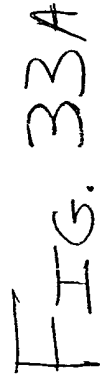
FIG. 28

LOGICAL (# ADDRESS WORDS)	Logical BITS	ASSUME 8 BITS/WORD	Physical BITS	PHYSICAL (# ADDRESS WORDS)
MAX/8 - 64K	MAX - 512K	MEM BLOCK D <sub>N</sub>	MAX	MAX/8
MAX/8 - 128K	MAX - 1024K	MEM BLOCK C <sub>N</sub>	MAX - 512K	MAX/8 - 64K
MAX/8 - 192K	MAX - 1536K	MEM BLOCK B <sub>N</sub>	MAX - 1024K	MAX/8 - 128K
MAX/8 - 256K	MAX - 2048K	MEM BLOCK A <sub>N</sub>	MAX - 1536K	MAX/8 - 192K
MAX/8 - 320K	MAX - 2560K		MAX - 2048K	MAX/8 - 256K
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
448K	3584K	MEM BLOCK D <sub>2</sub>	4096K	512K
384K	3072K	MEM BLOCK C <sub>2</sub>	3584K	448K
320K	2560K	MEM BLOCK B <sub>2</sub>	3072K	384K
256K	2048K	MEM BLOCK A <sub>2</sub>	2560K	320K
192K	1536K	MEM BLOCK D <sub>1</sub>	2048K	256K
(192K - 1)	(1536K - 1)	MEM BLOCK C <sub>1</sub>	(2048K - 1)	(256K - 1)
128K	1024K	MEM BLOCK B <sub>1</sub>	1536K	192K
64K	512K	MEM BLOCK A <sub>1</sub>	1024K	128K
OK	OK		512K	64K
			OK	OK

FIG. 29







209115

2719AA-2719NN

2718AA-2718NN

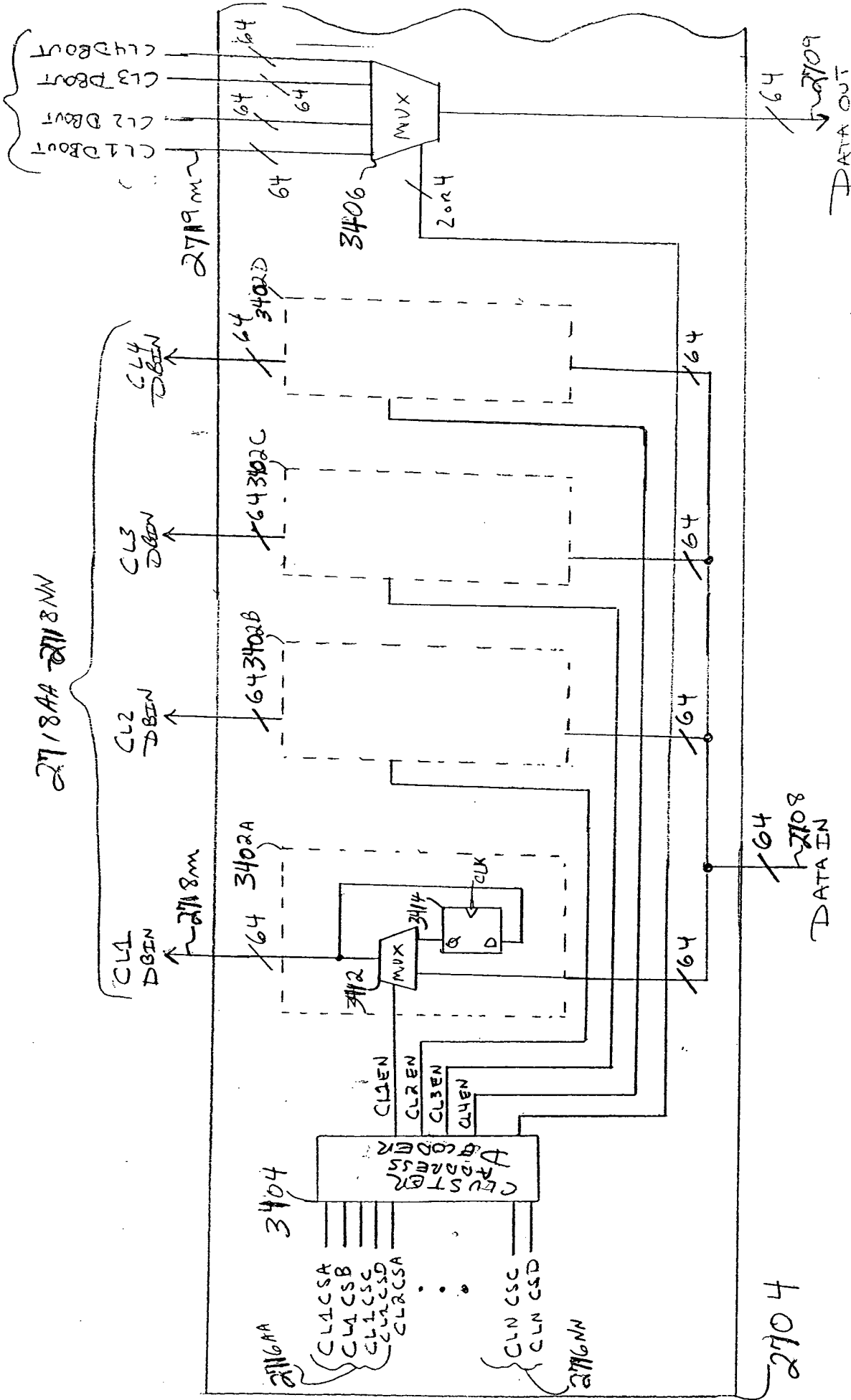


FIG. 33B

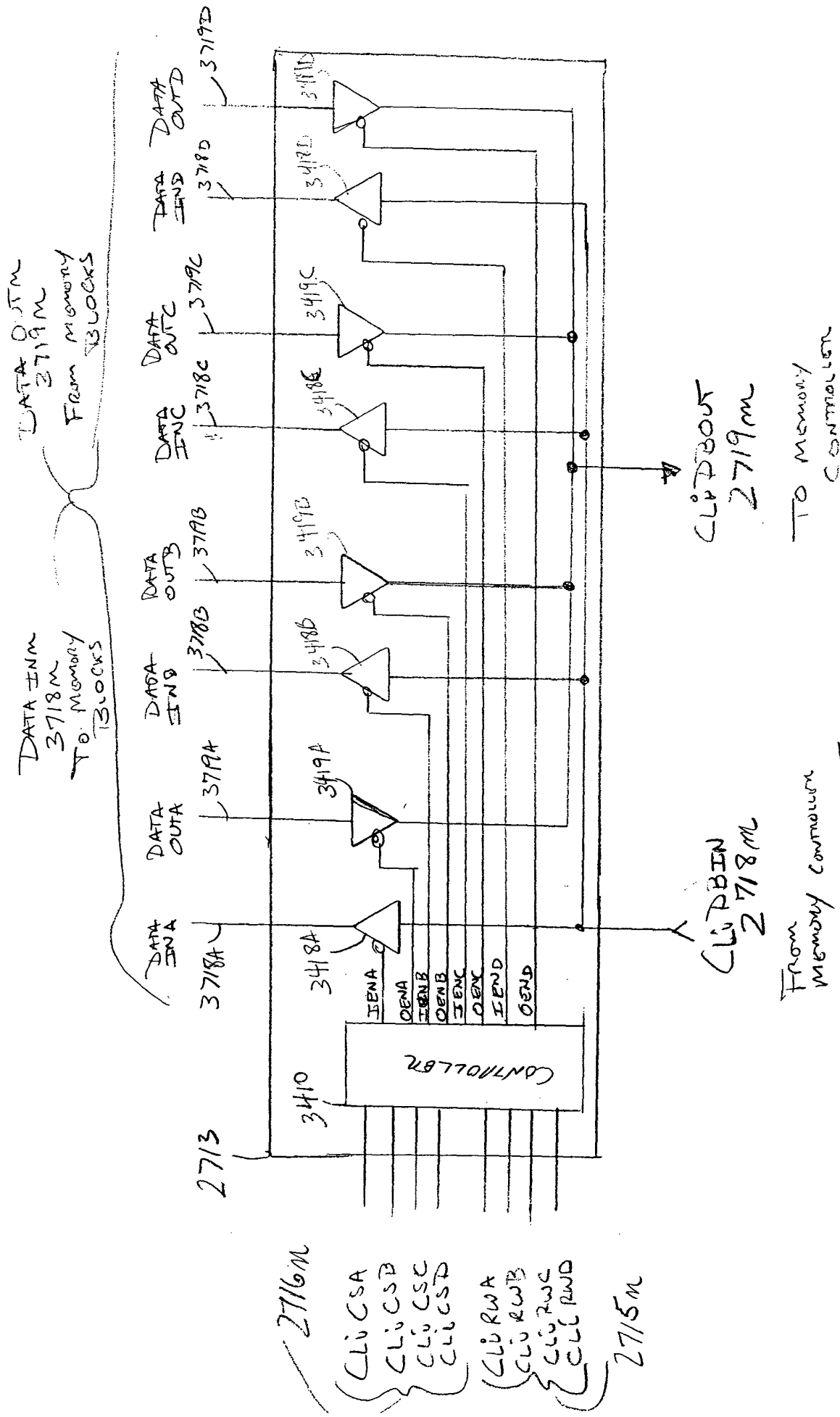


FIG. 34

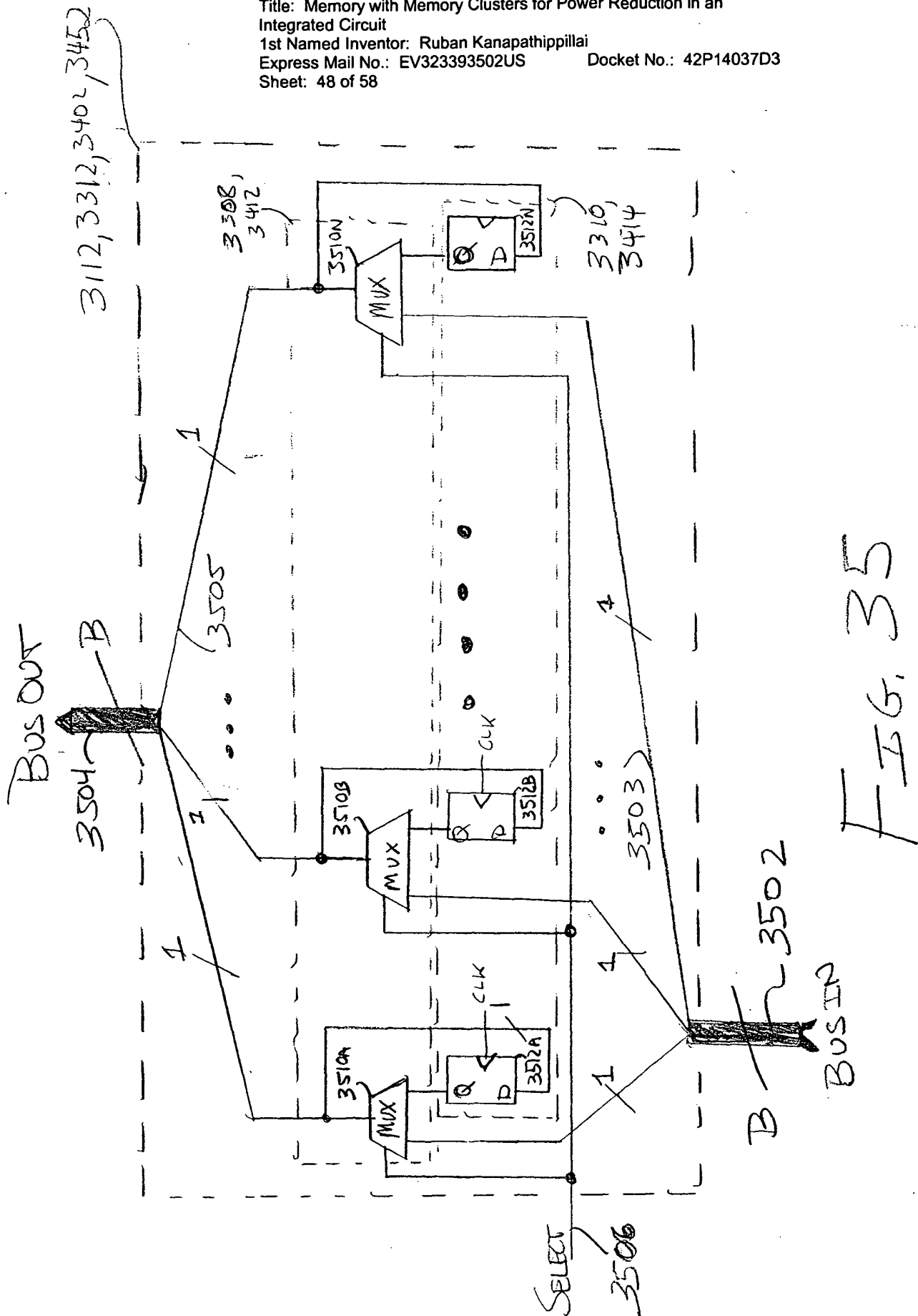


FIG. 35



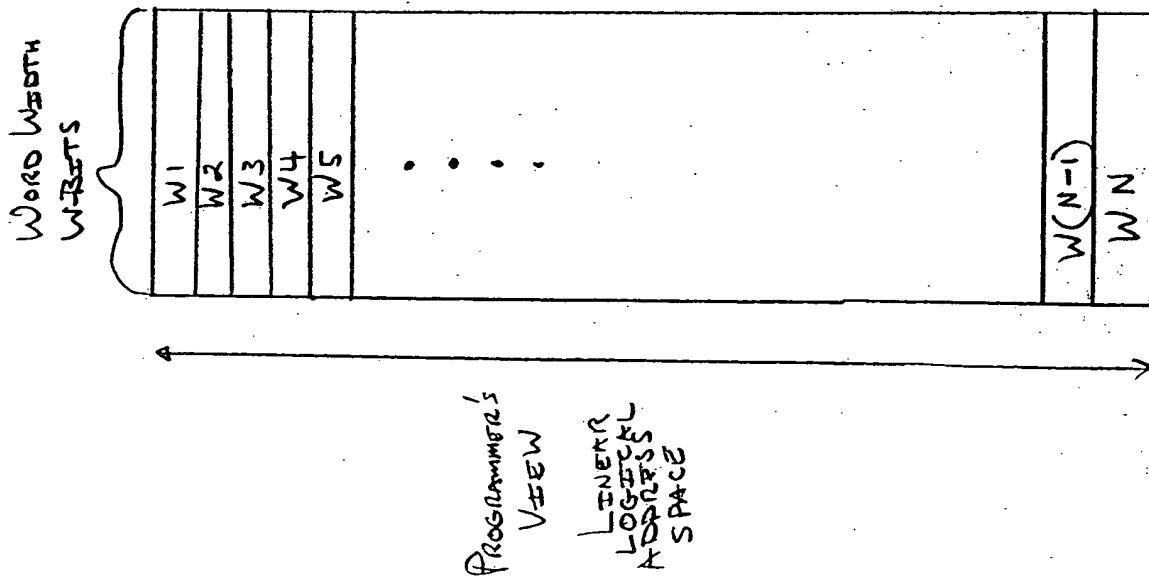
202

3604L				3604R			
WLN					FF...F	RWLN	
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
WL4	18	19	1A	1C	1E	1F	RWL4
WL3	10	11	12	14	16	17	RWL3
WL2	08	09	0A	0C	0E	0F	RWL2
WL1	00	01	02	04	06	07	RWL1
	LWBC1	LWBC2	LWBC3	LWBC4	RWBC3	RWBC4	

SEQUENCE # START ADDRESS

3602  
 OF F BOUNDARY ROW  
 ADDRESS DECODER

FIG. 36A



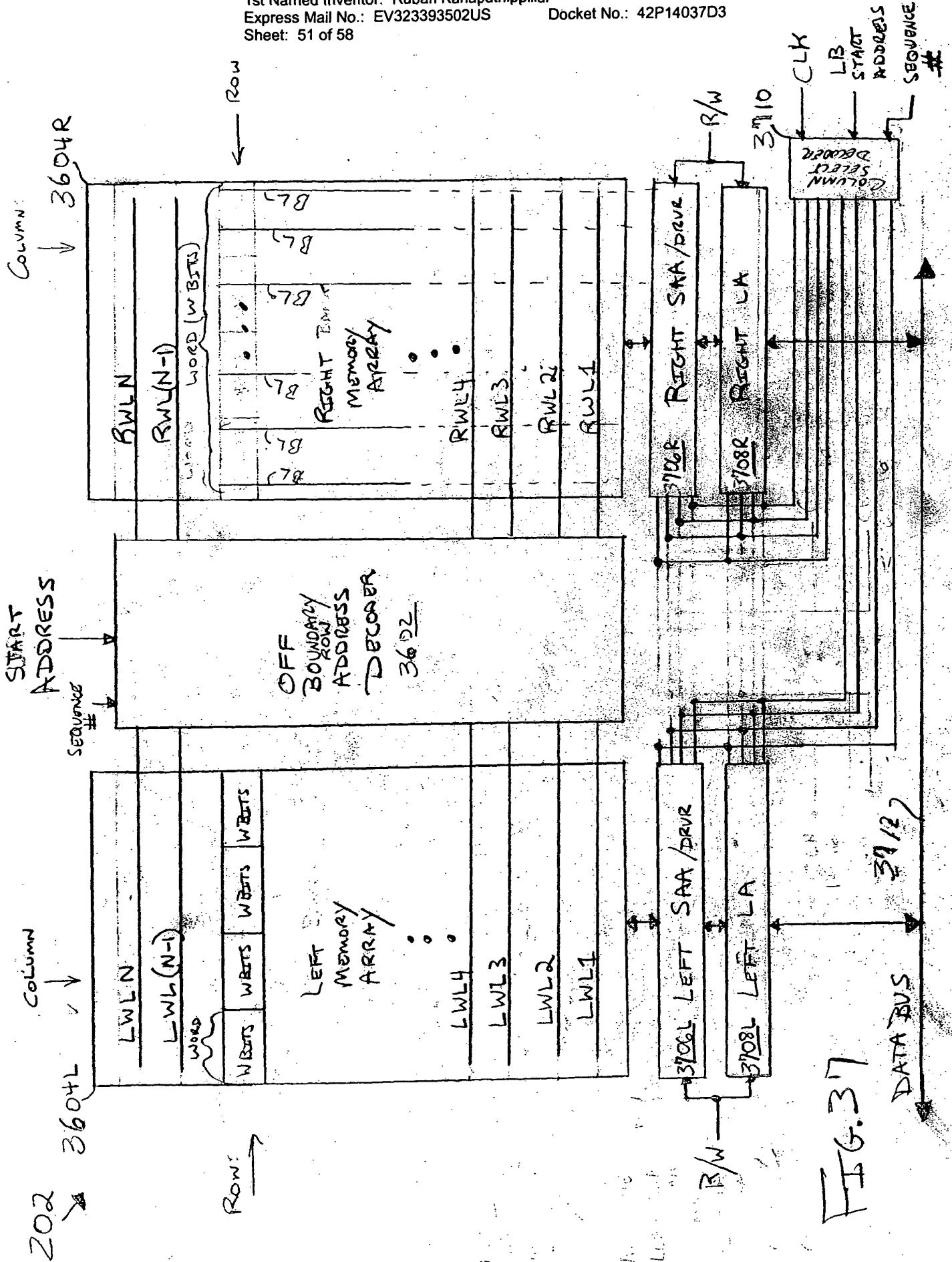
00	01	10	11
	$W1$	$W2$	$W3$
$W4$	.	.	.
		$W(N-1)$	$WN$

HARDWARE DESIGNER'S VIEW

OFFSET PHYSICAL ADDRESS SPACE

FIG. 36C

FIG. 36B



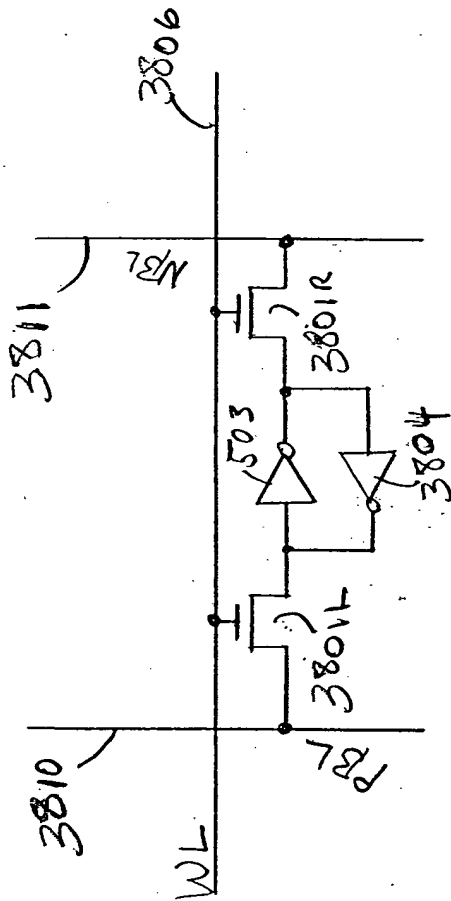


FIG. 38A

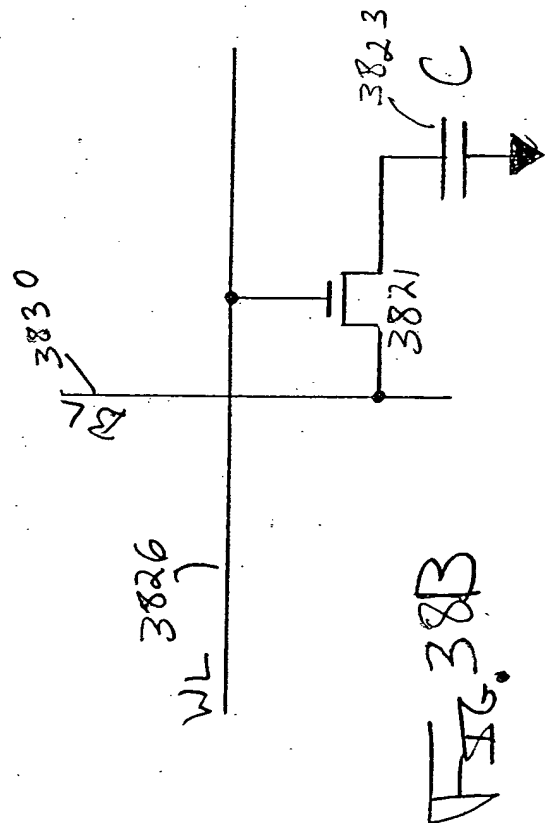
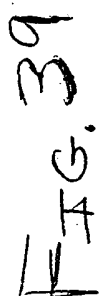


FIG. 38B



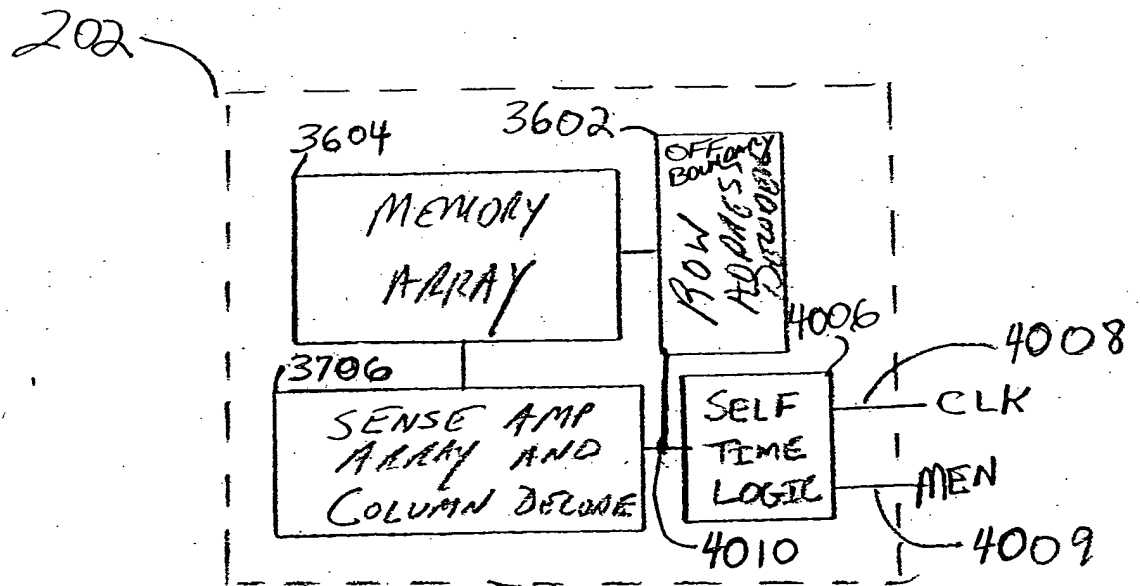


FIG. 40

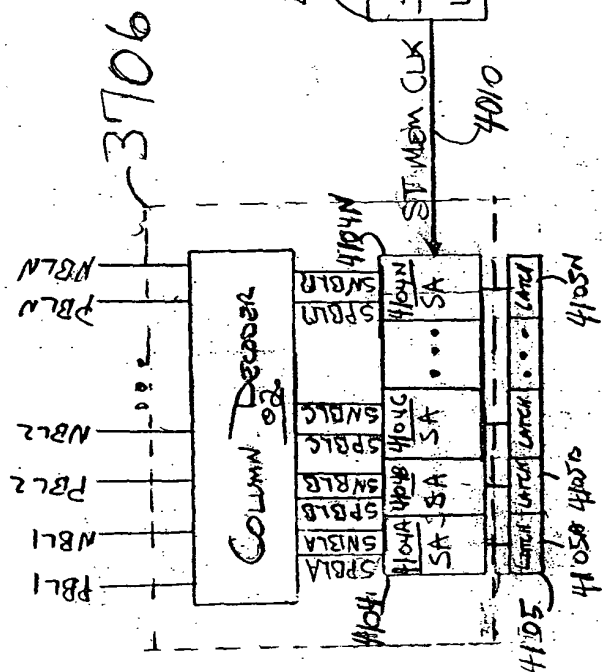


FIG. 41

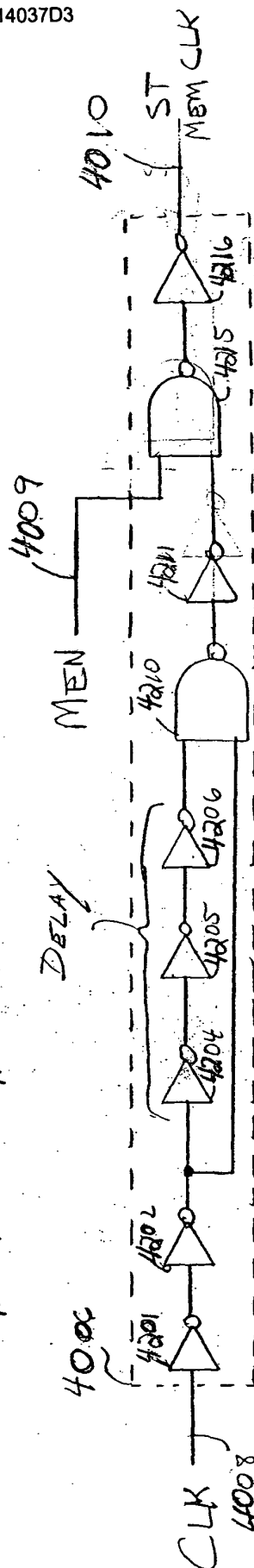


FIG. 42

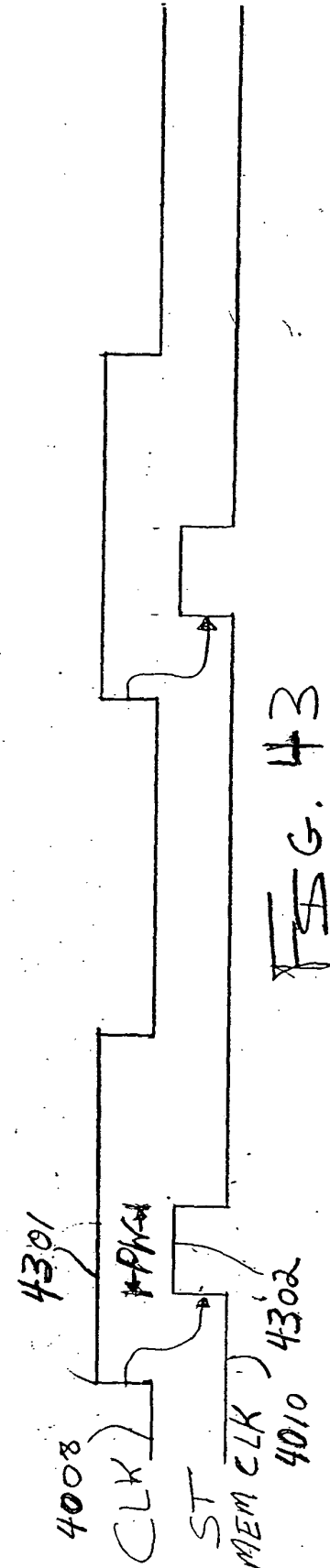


FIG. 43

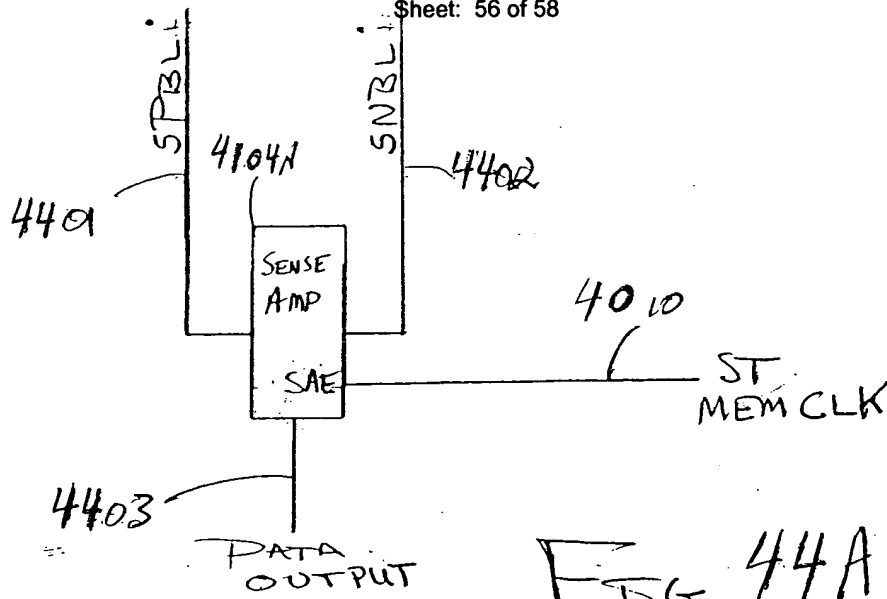


FIG. 44A

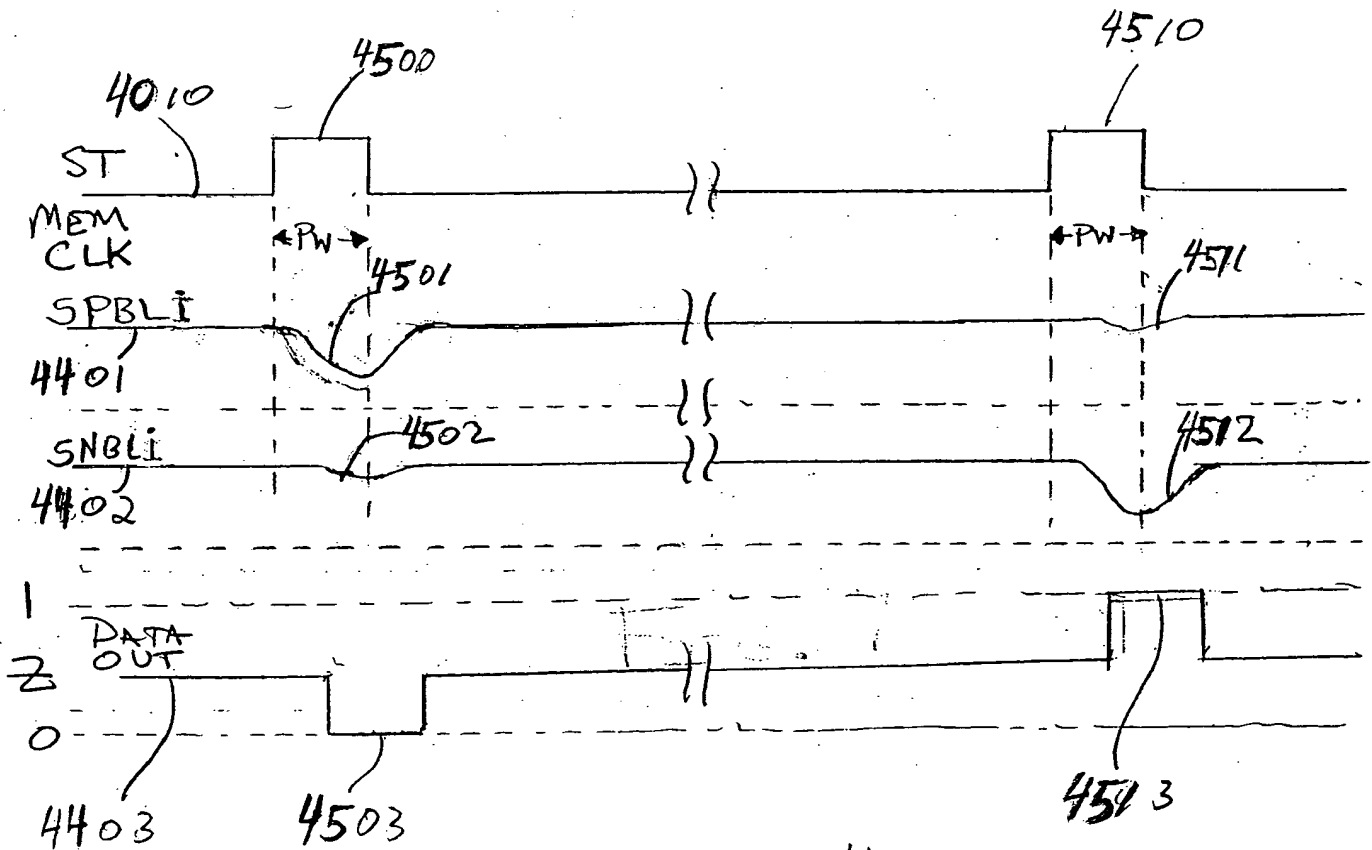
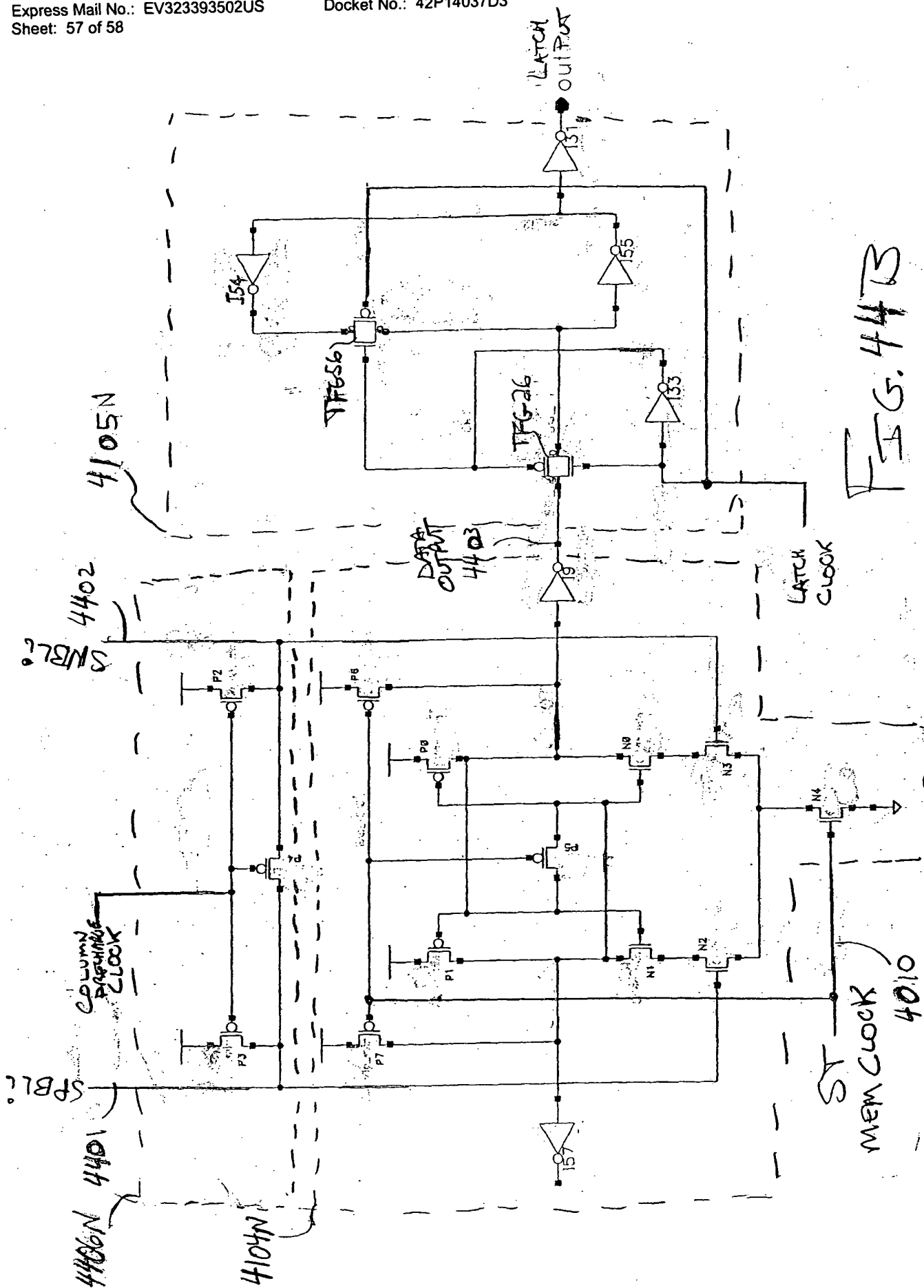
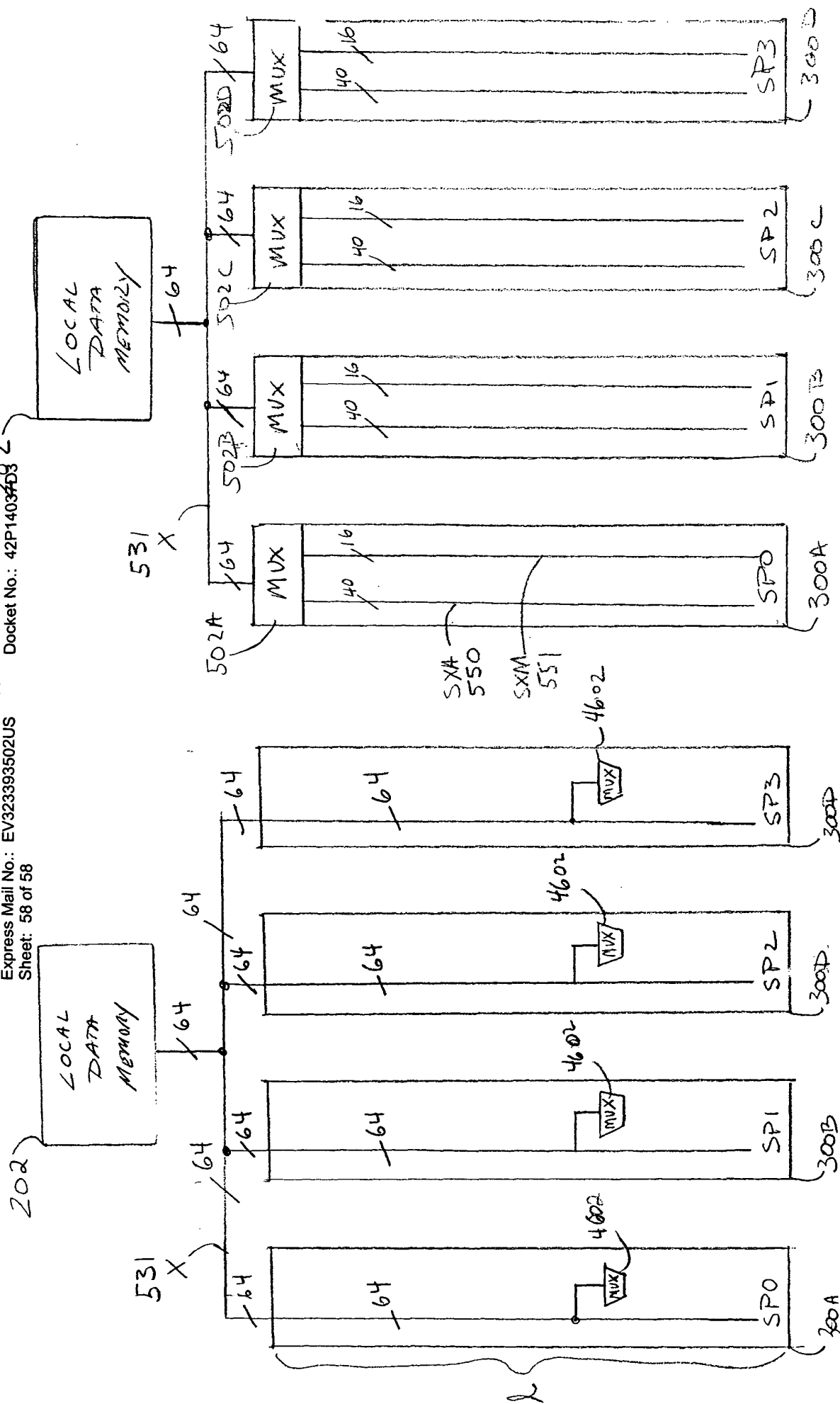


FIG. 45







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